2017

MADE EASY
WORKBOOK

Analog Electronics + Digital Electronics + Microprocessors

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Section-B Digital Electronics

Digital Electronics
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1 Number Systems and Binary Codes

Multiple Choice Questions

Q.1 What are the values respectively, of R_1 and R_2 in the expression $(235)_{R1} = (565)_{10} = (1065)_{R2}$?
(a) 8, 16 (b) 16, 8
(c) 6, 16 (d) 12, 8
[ESE-2004(EE)]

Q.2 $(2)_3 + (3)_4 = (?)_5$
(a) 4 (b) 11
(c) None of these (d) Not possible

Q.3 Convert the octal number 127543 into the hexadecimal form.
(a) AF63 (b) AF53
(c) AFD3 (d) BCD3

Q.4 If $(11x1y)_8 = (12C9)_{16}$ then the values x and y are
(a) 3 and 1 (b) 5 and 7
(c) 7 and 5 (d) 1 and 5
[ESE-2012]

Q.5 If $(2.3)_{base\ 4} + (1.2)_{base\ 4} = (y)_{base\ 4}$; what is the value of y?
(a) 10.1 (b) 10.01
(c) 10.2 (d) 1.02
[ESE-2005]

Q.6 How many 1's are present in the binary representation of
$(4 \times 4096) + (9 \times 256) + (7 \times 16) + 5$?
(a) 8 (b) 9
(c) 10 (d) 11 [ESE-2004]

Q.7 Which of the following represents '$E3_{16}$'?
(a) $(1CE)_{16} + (A2)_{16}$
(b) $(1BC)_{16} - (DE)_{16}$
(c) $(2BC)_{16} - (1DE)_{16}$
(d) $(200)_{16} - (11D)_{16}$ [ESE-2002]

Q.8 Which of the following subtraction operations result in F_{16}?
1. $(BA)_{16} - (AB)_{16}$
2. $(BC)_{16} - (CB)_{16}$
3. $(CB)_{16} - (BC)_{16}$

Select the correct answer using the code given below:
(a) Only 1 and 2 (b) Only 1 and 3
(c) Only 2 and 3 (d) 1, 2 and 3
[ESE-2006]

Q.9 The binary equivalent of hexadecimal number 4F2D.
(a) 0101 1111 0010 1100
(b) 0100 1111 0010 1100
(c) 0100 1110 0010 1101
(d) 0100 1111 0010 1101 [ESE-2002]

Q.10 $(FE35)_{16}$XOR$(CB15)_{16}$ is equal to
(a) $(3320)_{16}$ (b) $(FF35)_{16}$
(c) $(FF50)_{16}$ (d) $(3520)_{16}$
[ESE-2000]

Q.11 F's complement of $(2BFD)_{hex}$ is
(a) $E304$ (b) $D403$
(c) $D402$ (d) $C403$ [ESE-2001]

Q.12 The 2's complement representation of –17 is
(a) 101110 (b) 101111
(c) 111110 (d) 110001
[GATE-2001]

Q.13 The 2's complement representation $(-539)_{10}$ in hexadecimal is
(a) ABE (b) DBC
(c) DE5 (d) 9E7 **[GATE-2001]**

Q.14 In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)
(a) 0, 10110.1011 (b) 0, 10110.1001
(c) 1, 10101.1001 (d) 1, 10110.1001
[ESE-2002]

Q.15 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?
(a) 25, 9 and 57 respectively
(b) –6, –6 and –6 respectively
(c) –7, –7 and –7 respectively
(d) –25, –9 and –57 respectively
[GATE-2004]

Q.16 The range of signed decimal numbers that can be represented by 6-bit 1's complement number is
(a) –31 to +31 (b) –63 to + 63
(c) –64 to + 63 (d) –32 to + 31
[GATE-2004]

Q.17 Which of the following statement is **Incorrect** for the range of n bits binary numbers
(a) Range of unsigned numbers is 0 to $(2^n - 1)$
(b) Range of signed magnitude number is $-(2^{n-1} - 1)$ to $(2^{n-1} - 1)$
(c) Range of signed 1's compliment numbers is $(-2^{n-1} + 1)$ to (2^{n-1})
(d) Range of signed 2's compliment numbers is (-2^{n-1}) to $(2^{n-1} - 1)$

Q.18 A number in 4-bit 2's complement representation is $X_3 X_2 X_1 X_0$. This number when stored using 8-bits will be
(a) $0000\ X_3 X_2 X_1 X_0$
(b) $1111\ X_3 X_2 X_1 X_0$
(c) $X_3 X_3 X_3 X_3 X_3 X_2 X_1 X_0$
(d) $1\ X_3 X_3 X_3 X_3 X_2 X_1 X_0$ **[GATE-1999]**

Q.19 Two 4-bit 2's complement numbers 1011 and 0110 are added. The result expressed in 4-bit 2's complement notation is
(a) 0001
(b) 0010
(c) 1101
(d) cannot be expressed in 4-bit 2's complement
[GATE-IN:2003]

Q.20 Which of the following is an invalid state in 8-4-2-1 Binary Coded Decimal counter
(a) 1 0 0 0 (b) 1 0 0 1
(c) 0 0 1 1 (d) 1 1 0 0
[GATE-2014]

Q.21 The *BCD* code for a decimal number $(874)_{10}$ is
(a) $(100001110100)_{BCD}$
(b) $(010001111000)_{BCD}$
(c) $(100001000111)_{BCD}$
(d) $(011110000100)_{BCD}$
[ESE-2012]

Q.22 A decimal number 6 is written in excess-3 code as
(a) 0110 (b) 0011
(c) 1101 (d) 1001

Q.23 Which of the following weighted code will give 9's complement by changing (complementing) each individual bit?
(a) Excess-3 (b) 5421
(c) 2421 (d) Both (a) and (c)

Q.24 What is the Gray code word for the binary binary 101011?
(a) 101011 (b) 110101
(c) 011111 (d) 111110
[ESE-2006]

Numerical Data Type Questions

Q.25 The minimum decimal equivalent of the number 11C.0 is _____.
[ESE-2000]

Q.26 The decimal equivalent of hexadecimal number of 2A0F is _____.
[ESE-2002(EE)]

Q.27 The decimal equivalent of binary number 10110.11 is_____.

Q.28 In a particular number system having base B. $(\sqrt{41})_B = 5_{10}$. The value of 'B' is _____.

Q.29 $(-64)_{10} + (80)_{16} = (?)_{10}$
[ESE-2007]

Q.30 Given $(135)_{\text{base x}} + (144)_{\text{base x}} = (323)_{\text{base x}}$
The value of base x is _____.
[ESE-2005]

Q.31 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is _____.
[GATE-1993]

Q.32 A number is expressed in binary two's complement as 10011. Its decimal equivalent value is _____.
[ESE-2002]

Q.33 $(X)_8$ is expressed in gray code as $(11110)_2$. The value of X is_____.

Q.34 Consider a system which has two eight bit inputs D_1 = 01010101, D_2 = 00000000, the system produces eight bit output that is bitwise XOR of the inputs. The eight bit output of the system is input to the Gray Code Converter, the decimal equivalent of the output from Gray Code Converter is _____.

Q.35 The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is ____.
[GATE-2016]

Try Yourself

T1. Find the value of x.
$(135)_x + (144)_8 = (214)_{x+2}$
[Ans: $x = 7$]

T2. Consider the addition of numbers with different bases
$(X)_7 + (Y)_8 + (W)_{10} + (Z)_5 = (K)_9$
If $X = 36$, $Y = 67$, $W = 98$ and $K = 241$ then find the value of Z.
[Ans: 34]

T3. For radix r, decimal value of $(110)_r$ is $4r$ then r is _____ and decimal value of $(010)_r$ is ____ .

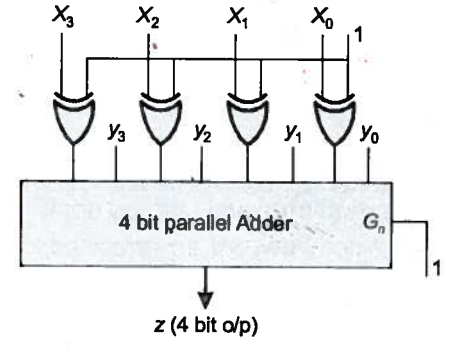
T4. If $(10)_x \times (10)_x = (100)_x$; $(100)_x \times (100)_x = (10000)_x$ then x can take value:
(a) 2 (b) 5
(c) 10 (d) All of these

T5. Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____.
[GATE-2014, Ans: (3)]

T6. If 73_x (in base-x number system) is equal to 54_y (in base-y number system), the possible values of x and y are
(a) 8, 16 (b) 10, 12
(c) 9, 13 (d) 8, 11
[GATE-2004, Ans: (d)]

T7. Consider the following multiplication:
$(10w1z)_2 \times (15)_{10} = (y01011001)_2$
Which one of the following gives appropriate values of w, y and z?
(a) $w = 0, y = 0, z = 1$
(b) $w = 0, y = 1, z = 1$
(c) $w = 1, y = 1, z = 1$
(d) $w = 1, y = 1, z = 0$
[ESE-2004(EE)]

T8. Identify the correct statement with respect to following circuit? Numbers are represented in signed magnitude format.



(a) It outputs $x + y$ (b) It outputs $y - x$
(c) It outputs $x + 1$ (d) It outpus $y + 1$

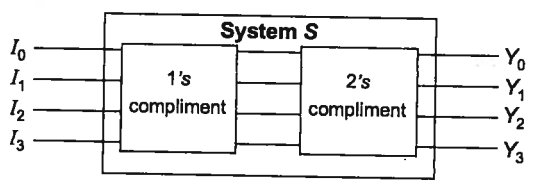
T9. An equivalent 2's complement representation of the 2's complement number 1101 is
(a) 110100 (b) 001101
(c) 110111 (d) 111101
[GATE-1998, Ans: (d)]

T10. Twos complement format of + 127 is
(a) 01111111 (b) 10000000
(c) 01101101 (d) 10010010
[Ans: (a)]

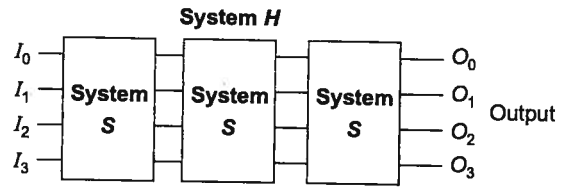
T11. The number of 1's in 8-bits representation of –127 in 2's complement form is m and that in 1's complement form is n. What is the value of m / n?
[ESE-2005]

T12. The range of integers that can be represented by an n-bit 2's complement number system is_____.
(a) -2^{n-1} to $(2^{n-1} - 1)$
(b) $-(2^{n-1} - 1)$ to $(2^{n-1} - 1)$
(c) $-(2^{n-1} + 1)$ to 2^{n-1}
(d) $-(2^{n-1} + 1)$ to $(2^{n-1} - 1)$
[ISRO-2009, Ans: (a)]

T13. Consider a **System *S*** as shown in the figure below

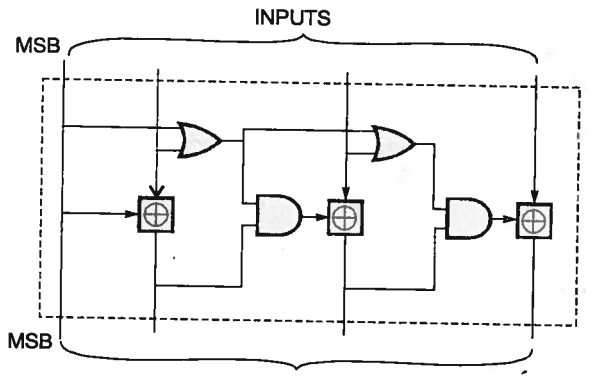


System *S* performs 1's compliment of the input and then 2's compliment to produce output.
A new **System *H*** is designed in which 3 **System *S*** are cascaded.



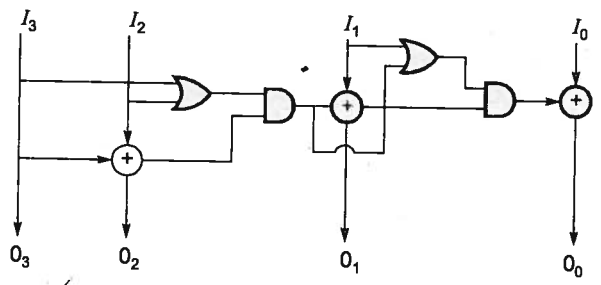
If the applied input $(I_3 I_2 I_1 I_0)$ is 1010, then what is the output $(O_3 O_2 O_1 O_0)$.
[Ans: 1101]

T14. The circuit shown in the figure converts



(a) BCD to binary code
(b) Binary to excess - 3 code
(c) Excess - 3 to Gray code
(d) Gray to Binary code

T15. The circuit shown below converts. (here ⊕ is XOR)



(a) Binary to gray
(b) Binary to Excess 3
(c) Excess 3 to gray
(d) Gray to binary

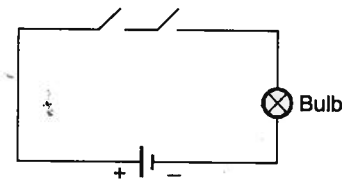
T16. Write gray code for binary numbers from 0000 to 1111.

2 Boolean Algebra, Logic Gates and K-Maps

Multiple Choice Questions

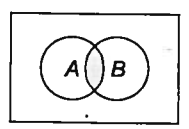
Q.1 The precedence order while solving Boolean expression is
(a) ( ) < OR < AND < NOT
(b) ( ) > NOT > AND > OR
(c) ( ) < NOT < AND < OR
(d) ( ) < AND > NOT > OR

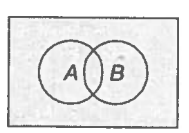
Q.2 What logic gate is represented by the circuit shown below?

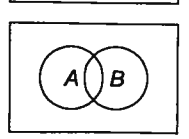


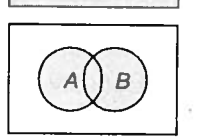
(a) AND (b) NAND
(c) NOR (d) EQUIVALENCE

Q.3 The expression $A + \bar{A}B$ is represented by

(a) 

(b) 

(c) 

(d) 

Q.4 If $X = 1$ in the logic equation
$\left[X + Z\left\{\bar{Y} + (\bar{Z} + X\bar{Y})\right\}\right]\left\{\bar{X} + \bar{Z}(X + Y)\right\} = 1$ then
(a) $Y = Z$ (b) $Y = \bar{Z}$
(c) $Z = 0$ (d) $Z = 1$
[GATE-2009]

Q.5 The Boolean expression
$ABCD + A\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D}$
is equivalent to
(a) A (b) AC
(c) ABC (d) 1
[ESE-2008]

Q.6 If x and y are Boolean variables, which one of the following is the equivalent of $x \oplus y \oplus xy$?
(a) $x + \bar{y}$ (b) $x + y$
(c) 0 (d) 1
[ESE-2004(EE)]

Q.7 The Boolean expression $\bar{Y}\bar{Z} + \bar{X}\bar{Y} + \bar{X}\bar{Z}$ is logically equivalent to
(a) $YZ + \bar{X}$
(b) $X\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z$
(c) $XYZ + \bar{X}\bar{Y}\bar{Z}$
(d) $XY + YZ + XZ$

Q.8 The total number of Boolean functions that can be constructed for n Boolean variables is
(a) n (b) 2^n
(c) $(2^n)^n$ (d) 2^{2n}
[DRDO-2009]

Q.9 With 4 Boolean variables, how many Boolean expressions can be formed?
(a) 16 (b) 256
(c) 1024 (1 K) (d) 64 K (64 × 1024)
[ESE-2002]

Q.10 Consider the statement below:
1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement, which is always true, is
(a) Both 1 and 2 (b) Only 1
(c) Only 2 (d) None of these

Q.11 If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either
(a) A NAND or A NOR
(b) An AND or an EX-NOR
(c) An OR or an NAND
(d) An EX-OR or an EX-NOR **[ESE-2014]**

Q.12 Which one of the following statements is correct?
For a 4-input NOR gate, when only two inputs are to be used, the best option for the unused inputs is to
(a) connect them to the ground
(b) connect them to V_{CC}
(c) keep them open
(d) connect them to the used inputs
[ESE-2004(EE)]

Q.13 How is inversion achieved using EX-OR gate?
(a) Giving input signal to the two input lines of the gate tied together.
(b) Giving input to one input line and logic zero to the other line.
(c) Giving input to one input line and logic one to the other line.
(d) Inversion cannot be achieved using EX-OR gate.
[ESE-2002]

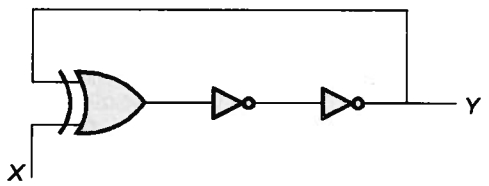
Q.14 Consider:
$Y = A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A$ the Y is equivalent to:
(a) 1 OR E (b) A EX OR 0
(c) 1 NOR B (d) A AND A

Q.15 The function
$f = \left(A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC + \bar{A}\bar{B}C\right) \oplus A$ can be written as:
(a) $B \oplus C$ (b) $A \oplus B \oplus A$
(c) A (d) None of these

Q.16 $\left[(A + A\bar{B})(A + \bar{A}\bar{B})\right] + \left[(CD + \bar{C}\bar{D}) + (C \oplus D)\right] =$
(a) B (b) A
(c) 0 (d) 1

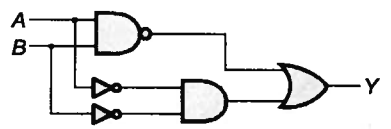
Q.17 **Statement (I):** XOR gate is not a universal gate.
Statement (II): It is not possible to realize any Boolean function using XOR gates only.
(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
(c) Statement (I) is true but Statement (II) is false.
(d) Statement (I) is false but Statement (II) is true.
[ESE-2012]

Q.18 All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



(a) $X = 0$ (b) $X = 1$
(c) $X = 0$ or 1 (d) $X = Y$
[GATE-IN:2006]

Q.19 The logic circuit of figure is a

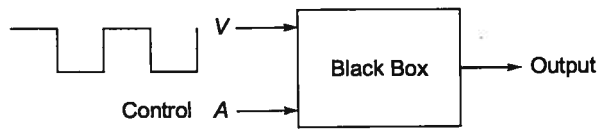


(a) Half adder (b) XOR
(c) Equality detector (d) NAND
[GATE-2003]

Q.20 If a variable is having Ex-OR operation itself 'n' number of times, then the result is
(a) Complement of variable if 'n' is even.
(b) Uncomplement of variable if 'n' is even.
(c) Complement of the variable if 'n' is odd.
(d) Uncomplement of the variable if 'n' is odd.

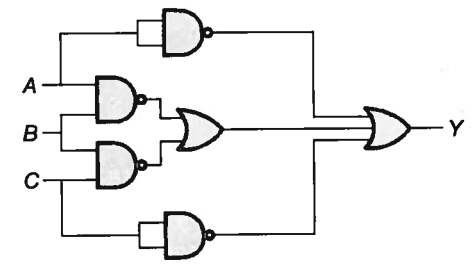
Q.21 An odd function involving three Boolean variables is
(a) $\Sigma(1, 3, 5, 7)$ (b) $\Sigma(0, 2, 4, 6)$
(c) $\Sigma(1, 2, 4, 7)$ (d) $\Sigma(0, 3, 5, 6)$
[DRDO-2009]

Q.22 Black box inverts the phase of input V when control 'A' is 1 and lets it pass through uninverted when control 'A' is 0 then circuit is



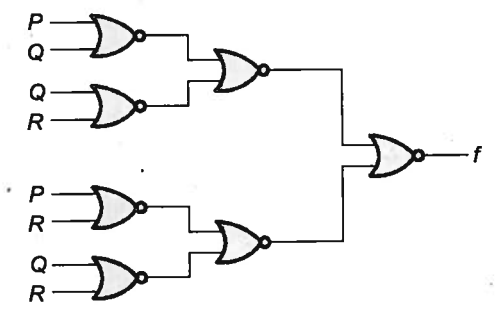
(a) XNOR gate (b) XOR gate
(c) NAND gate (d) NOR gate

Q.23 For the logic circuit shown in figure below, the output 'Y' is equal to



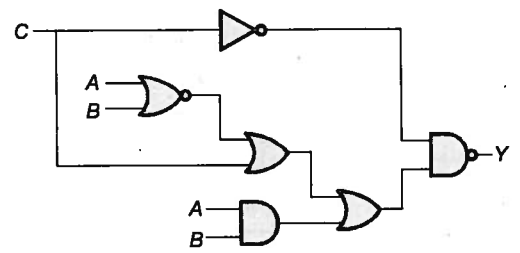
(a) $\overline{AB} + \overline{BC} + \bar{B} + \bar{C}$ (b) $\overline{AB} + \overline{BC}$
(c) $\bar{A} + \bar{B} + \bar{C}$ (d) All of these

Q.24 What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below?



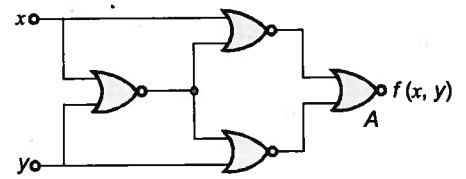
(a) $\overline{Q + R}$ (b) $\overline{P + Q}$
(c) $\overline{P + R}$ (d) $\overline{P + Q + R}$
[GATE-2010]

Q.25 In the circuit shown in the figure, if $C = 0$, the expression for Y is



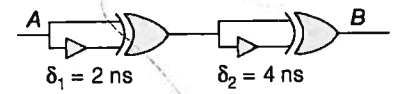
(a) $Y = A\bar{B} + \bar{A}B$ (b) $Y = A + B$
(c) $Y = \bar{A} + \bar{B}$ (d) $Y = AB$
[GATE-2014]

Q.26 Identify the logic function performed by the circuit shown

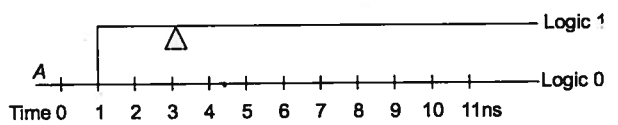


(a) Exclusive OR (b) Exclusive NOR
(c) NAND (d) NOR
[GATE-1993]

Q.27 Consider the following circuit composed of XOR gates and non-inverting buffers.



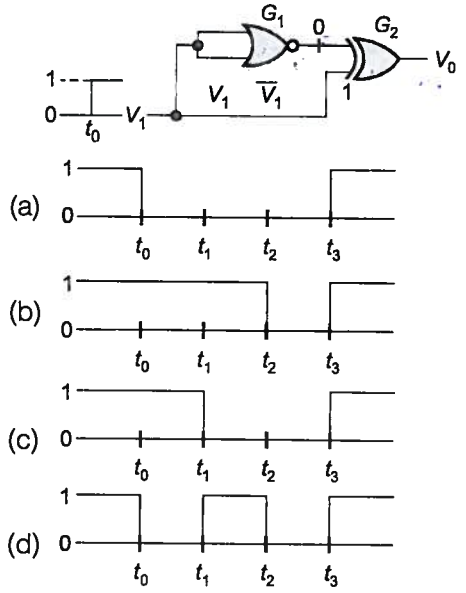
The non-inverting buffers have delays $d_1 = 2$ ns and $d_2 = 4$ ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns



(a) 1 (b) 2
(c) 3 (d) 4
[GATE-2003]

Q.28 The gates G_1 and G_2 in the figure have propagation delays of 10 nsec and 20 nsec respectively. If the input V_i makes an abrupt

change from logic 0 to 1 at time $t = t_0$, then the output waveform V_0 is
($t_1 = t_0 + 10$ ns, $t_2 = t_0 + 20$ ns, $t_3 = t_0 + 30$ ns)



[GATE-2002]

Q.29 The switching expression corresponding to $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$ is
(a) $BC'D' + A'C'D + AB'D$
(b) $ABC' + ACD + B'C'D$
(c) $ACD' + A'B'C' + AC'D'$
(d) $A'BD + ACD' + BCD'$

[ISRO-2009]

Q.30 The Boolean expression $AC + B\bar{C}$ is equivalent to
(a) $\bar{A}C + B\bar{C} + AC$
(b) $\bar{B}C + AC + B\bar{C} + \bar{A}C\bar{B}$
(c) $AC + B\bar{C} + \bar{B}C + ABC$
(d) $ABC + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}C$

[GATE-EC:2004]

Q.31 What is the minimized logic expression corresponding to the given Karnaugh Map?

wx \ yz	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

(a) xz
(b) $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}\bar{z} + wxy$
(c) $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}\,\bar{z} + wx\bar{y}$
(d) $xz + \bar{w}yz + \bar{w}x\bar{y} + wxy + w\bar{y}z$

[ESE-2005]

Q.32 The function $f(A, B, C, D) = \Sigma(5, 7, 9, 11, 13, 15)$ is independent of variable(s)
(a) B (b) C
(c) A and C (d) D

[DRDO-2009]

Q.33 Consider the following boolean function of four variables
$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$, The function is
(a) independent of one variable
(b) independent of two variables
(c) independent of three variables
(d) dependent on all the variables

[ISRO-2009]

Q.34 The min term of $f(P, Q, R) = PQ + QR' + PR'$ is
(a) $m_2 + m_4 + m_6 + m_7$
(b) $m_0 + m_1 + m_3 + m_5$
(c) $m_0 + m_1 + m_6 + m_7$
(d) $m_2 + m_3 + m_4 + m_5$

[GATE-2010]

Q.35 The Boolean functions can be expressed in canonical SOP (sum of products) and POS (product of sums) form. For the functions, $Y = A + \bar{B}C$, which are such two forms
(a) $Y = \Sigma(1,2,6,7)$ and $Y = \Pi(0, 2, 4)$
(b) $Y = \Sigma(1,4,5,6, 7)$ and $Y = \Pi(0, 2, 3)$
(c) $Y = \Sigma(1,2,5,6, 7)$ and $Y = \Pi(0, 1, 3)$
(d) $Y = \Sigma(1, 2, 4, 5, 6, 7)$ and $Y = \Pi(0, 2, 3, 4)$

[GATE-2008]

Q.36 The SOP (sum of products) form of a Boolean function is $\Sigma(0, 1, 3, 7, 11)$, where inputs are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is
(a) $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{B})(\bar{C} + D)$

(b) $(\bar{B} + C)(\bar{A} + C)(A + \bar{C})(\bar{C} + D)$
(c) $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + \bar{D})$
(d) $(\bar{B} + C)(A + \bar{B})(\bar{A} + \bar{B})(\bar{C} + D)$

[GATE-2014]

Q.37 What is the minimum number of NAND gates required to implement $A + A\bar{B} + \bar{B}C(A + \bar{C})$?
(a) 0 (b) 2
(c) 4 (d) 6

[GATE-2004]

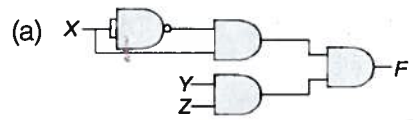
Linked Answer Questions (38 and 39):
The following Karnaugh map represents a function F.

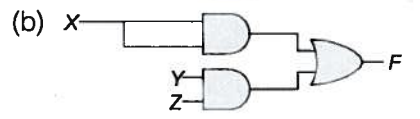
F, YZ \ X	00	01	11	10
0	1	1	1	0
1	0	0	1	0

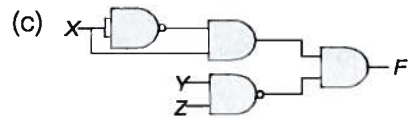
Q.38 A minimized form of the function F
(a) $F = \bar{X}Y + YZ$ (b) $F = \bar{X} \cdot \bar{Y} + YZ$
(c) $F = \overline{XY} + Y\bar{Z}$ (d) $F = \overline{XY} + \bar{Y}\bar{Z}$

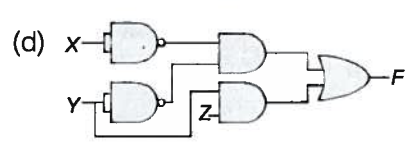
[GATE-2010]

Q.39 Which of the following circuits is a realization of the above function F?

(a) 

(b) 

(c) 

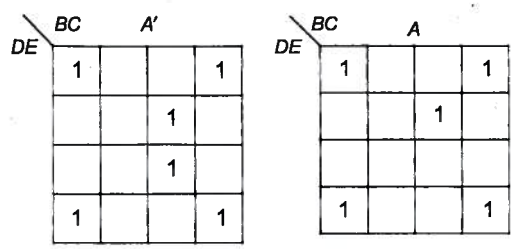
(d) 

[GATE-2010]

Q.40 The minterms for $AB + ACD$ are
(a) $\bar{A}\bar{B}CD + AB\bar{C}D + A\bar{B}C\bar{D} + A\bar{B}CD + \bar{A}BCD$
(b) $AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD + A\bar{B}CD$
(c) $A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + \bar{A}BCD + A\bar{B}C\bar{D}$
(d) $AB\bar{C}D + A\bar{B}CD + \bar{A}BCD + ABC\bar{D} + \overline{A\bar{B}}CD$

[ESE-2013]

Q.41 The minimized function f obtained from the K-map given below is



(a) $C'E' + A'BCE + BCD'E$
(b) $B'C'E' + A'BCE + ABCD'E + BC'E'$
(c) $C'E' + A'BCD + BCDE$
(d) $B'C'E + A'BCE + ABCD'E + BC'E$

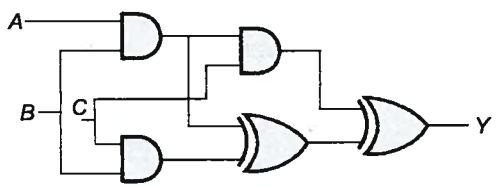
[DRDO-2008]

Q.42 Which are the essential prime implicants of the following Boolean function?
$f(a, b, c) = a'c + ac' + b'c$:
(a) $a'c$ and ac' (b) $a'c$ and $b'c$
(c) a' only (d) a' and bc'

[GATE-2004]

Q.43 Consider the Boolean function,
$F(w, x, y, z) = wy + xy + \bar{w}xyz + \bar{w}\bar{x}y + xz + \bar{x}\bar{y}\bar{z}$.
Which one of the following is the complete set of essential prime implicants?
(a) $w, y, xz, \bar{x}\bar{z}$ (b) w, y, xz
(c) $y, \bar{x}\bar{y}\bar{z}$ (d) $y, xz, \bar{x}\bar{z}$

Q.44 The output of the combinational circuit given below is



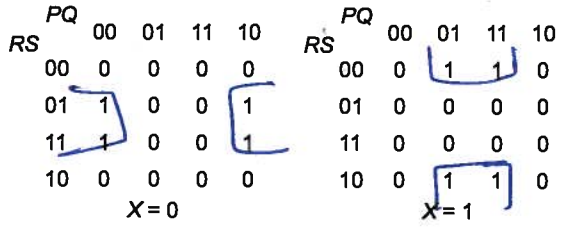
(a) $A + B + C$ (b) $A(B + C)$
(c) $B(C + A)$ (d) $C(A + B)$

[GATE-2016]

Q.45 The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is
(a) 4 (b) 5
(c) 6 (d) 7

[GATE-2016]

Q.46 Following is the *K*-map of a Boolean function of five variables *P*, *Q*, *R*, *S* and *X*. The minimum sum-of-product (SOP) expression for the function is



(a) $P\bar{Q}S\bar{X}+P\bar{Q}S\bar{X}+Q\bar{R}\bar{S}X+QR\bar{S}X$

(b) $\bar{Q}S\bar{X}+Q\bar{S}X$

(c) $\bar{Q}SX+Q\bar{S}\bar{X}$

(d) $\bar{Q}S+Q\bar{S}$

[GATE-2016]

Q.47 The chairman requested the aggrieved shareholders to _____ him.

(a) bare with (b) bore with

(c) bear with (d) bare

[GATE-2016]

Q.48 The Boolean expression $\overline{(a+\bar{b}+c+\bar{d})+(b+\bar{c})}$ simplifies is

(a) 1 (b) $\overline{a \cdot b}$

(c) a, b (d) 0

[GATE-2016]

Q.49 Consider the Boolean operator # with the following properties:

$x \# 0 = x, x \# 1 = \bar{x}, x \# x = 0$ and $x \# \bar{x} = 1$.

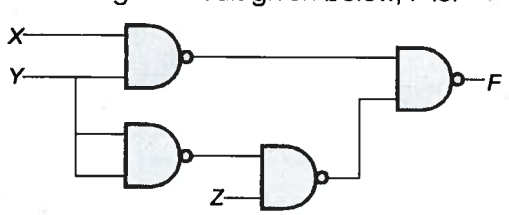
Then $x \# y$ is equivalent to

(a) $x\bar{y}+\bar{x}y$ (b) $\bar{x}\bar{y}+\bar{x}\,\bar{y}$

(c) $\bar{x}y+xy$ (d) $xy+\bar{x}\,\bar{y}$

[GATE-2016]

Q.50 In the digital circuit given below, *F* is:



(a) $XY+Y\bar{Z}$ (b) $XY+\bar{Y}Z$

(c) $\bar{X}\bar{Y}+Y\bar{Z}$ (d) $XZ+\bar{Y}$

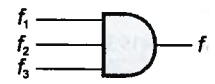
[GATE-2016]

Numerical Data Type Questions

Q.51 Consider the logical functions given below.

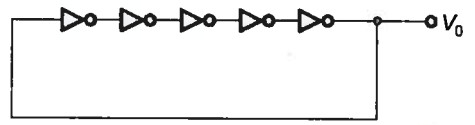
$f_1(A, B, C) = \Sigma(2, 3, 4)$

$f_2(A, B, C) = \pi(0, 1, 3, 6, 7)$

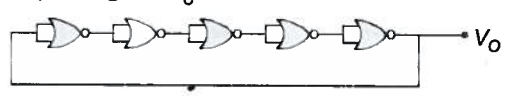


If *f* is logic zero, then maximum number of possible minterms in function f_3 are _____.

Q.52 For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency (in GHz) of the oscillator output?



Q.53 The average propagation delay of each NOR gate shown below is 10 ns. The frequency of the output signal V_0 is _____ MHz.



Q.54 The minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate is _____.

[GATE-2004]

Q.55 Minimum number of 2 input NAND gates required to implement the logic function $F = A + B + C + D$ are _____.

Q.56 The minimum number of 2 input NAND gates required to realize the Boolean function $f(A, B, C) = A\bar{B}C$.

Q.57 Consider the function:

$f = \bar{A}(\bar{B}C + BCD) + \bar{B}\bar{D}(A + C) + \bar{A}\bar{B}\bar{C}$

$d = \bar{A}B(C\bar{D} + \bar{C}D) + ACD$

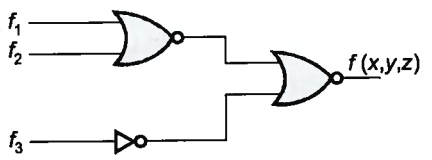
Where '*f*' represents Boolean function and '*d*' represents don't care condition.

Then simplified Boolean expression '*f*' is reduced to _____ literals.

Q.58 The number of prime-implicants for the given function $f(A, B, C) = \Sigma m(0, 2, 5, 6, 7)$ is ____.

Q.59 The number of essential prime-implicants in the given function $f(w, x, y, z) = \Sigma m(0, 2, 6, 7, 8, 9, 13, 15)$ is _____.

Try Yourself

T1. 

If $f_1(x, y, z) = \Sigma m(0, 1, 3, 5)$,

$f_2(x, y, z) = \Sigma m(4, 5)$ and

$f(x, y, z) = \Sigma m(1, 4, 5)$

then $f_3(x, y, z)$ is _____

(a) $\Sigma m(1, 4, 5)$

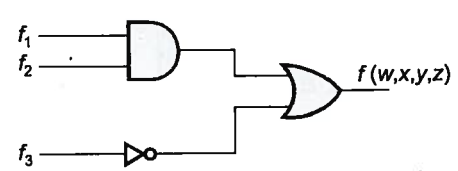
(b) $\Pi M(1, 4, 5)$

(c) $\Sigma m\{1, 4, 5) + d(2, 6, 7)$

(d) $\Pi M(1, 4, 5) \cdot d(2, 6, 7)$

[Ans: (c)]

T2. Determine the function f_3 if $f_1 = w\bar{x}z + y\bar{z} + x\bar{z}$ and the overall transmission function of the given logic circuit is to be $f(w, x, y, z) = \Sigma m(1, 3, 5, 6, 9, 12, 13)$



(a) $f_3 = \Sigma m(0, 2, 4, 7, 8, 10, 11, 14, 15)$

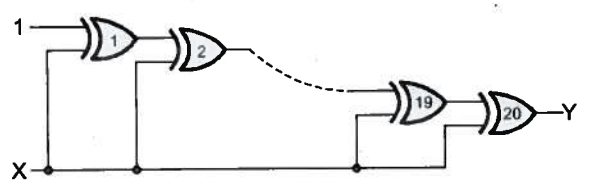
(b) $f_3 = \Sigma m(6, 9, 12)$

(c) $f_3 = \Sigma m(0,2,4,7,8,10,11,14,15) + d(6, 9,12)$

(d) $f_3 = \Sigma m(6, 9, 12) + d(0, 2, 4, 7, 8, 10, 11, 14, 15)$

[Ans: (c)]

T3. In input to digital circuit consisting of a cascade of 20 EXOR gates is '*X*' then output '*Y*' is:



(a) 0 (b) 1

(c) $\bar{X}$ (d) X

[Ans: (b)]

T4. Define the connective * for the Boolean variables X and Y as $X * Y = XY + X'Y'$. Let $Z = X * Y$. Consider the following expressions P, Q and R.

P : X = Y * Z

Q : Y = X * Z

R : X * Y * Z = 1

Which of the following is TRUE?

(a) Only P and Q are valid

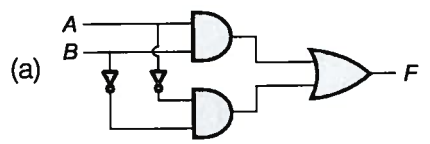
(b) Only Q and R are valid

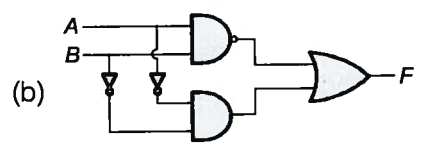
(c) Only P and R are valid

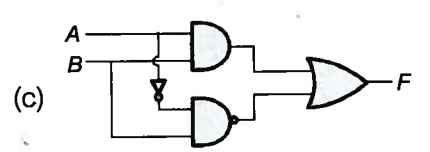
(d) All P, Q, R are valid.

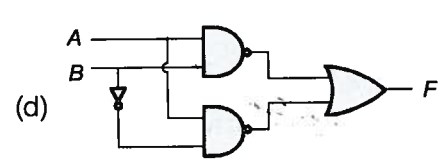
[GATE-2007, Ans: (d)]

T5. Which one of the following figures represents the coincidence logic?

(a) 

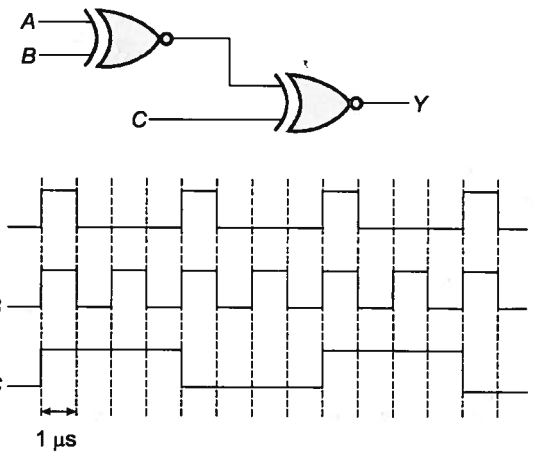
(b) 

(c) 

(d) 

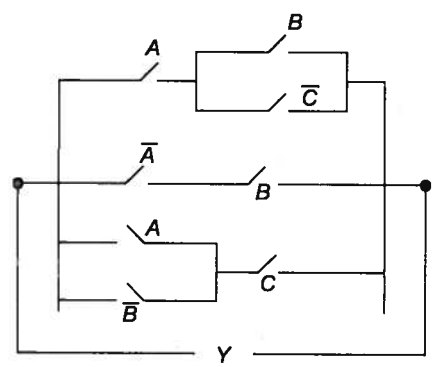
[ESE-2000]

T6. If the waveforms *A*, *B*, *C* shown in figure below are applied to the Ex-NOR gates. Find the frequency of output.



[Ans: 125 kHz]

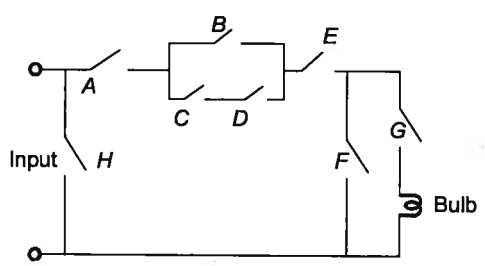
T7. Minimized expression for *Y* is



(a) $A + B + C$ (b) $A + BC$

(c) $A+\overline{B}C$ (d) $\overline{A}+\overline{B}+\overline{C}$

T8. A switching circuit is given below. Based on this circuit find the Boolean expression for the bulb.



T9. A Boolean function f of two variables *x* and *y* is defined as follows:

$f(0, 0) = f(0, 1) = f(1, 1) = 1$; $f(1, 0) = 0$

Assuming complements of *x* and *y* are not available, a minimum cost solution for realizing *f* using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

(a) 1 unit (b) 4 unit

(c) 3 unit (d) 2 unit **[GATE-2004]**

T10. *A T* gate is having the output $T(A, B) = \overline{A}B$. Which of the following is/are have about *T* gate.

(a) $\{T\}$ is functionally complete

(b) $\{T, 1\}$ is functionally complete

(c) $\{T, 0\}$ is functionally complete

(d) both a and b

[Ans: (b)]

T11. The simplification of Boolean expressions.

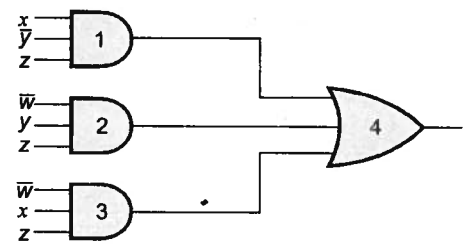
$a+\overline{a}b+\overline{a}\overline{b}c+....$ is

(a) $a+\overline{b}+\overline{c}+...$ (b) $\overline{a}+b+\overline{c}+...$

(c) $a+b+\overline{c}+...$ (d) $a + b + c + ...$

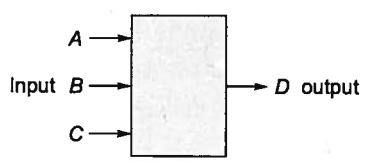
[Ans: (d)]

T12. The following labelled 1, 2, 3 and 4 in the network shown in the figure is redundant _____.



[ESE-1999]

T13. For the box shown the output *D* is true if and only if a majority of the inputs are true.



The Boolean function for the output is

(a) $D = AB\overline{C} + \overline{A}BC + A\overline{B}C$

(b) $D = ABC + \overline{A}BC + A\overline{B}C + AB\overline{C}$

(c) $D = \overline{A}\overline{B}\overline{C} + AB + AC + BC$

(d) $D = \overline{A}\overline{B}C + A\overline{B}\overline{C} + \overline{A}B\overline{C} + ABC$

[ESE-2013]

T14. What is the Boolean expression for the truth table shown below?

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
f	0	0	0	1	0	0	1	0

(a) $B(A+C)(\overline{A}+\overline{C})$

(b) $B(A+\overline{C})(\overline{A}+C)$

(c) $\overline{B}(A+C)(\overline{A}+C)$

(d) $\overline{B}(A+C)(\overline{A}+\overline{C})$

[GATE-2006]

T15. A bank has 3 locks with 1 key for each lock. Each key is owned by a different person. In order to open the vault atleast two people must insert their keys into the assigned locks. All the keys are not inserted at the same time. If the system is to be designed with only two input NAND gates, then find the number of NAND gates required.

[Ans: 6]

T16. A logic circuit implements the following Boolean function:

$F(A, B, C, D) = \overline{A}C + A\overline{C}D$

It is found that *m* the circuit the input combination $A = C$ can never occur. Find a simpler expression for *F*.

[ESE-2014]

T17. The standard sum of products of the function $f = A + B'C$ is expressed as:

(a) $\Sigma m(1, 4, 5, 6, 7) + d(, 2, 3)$

(b) $\Sigma m(1, 4, 5, 6, 7)$

(c) $\Sigma m(0, 2, 3) + d(1, 4, 5, 6, 7)$

(d) $\Pi M(1, 4, 5, 6, 7)$

[DRDO-2008]

T18. The black box in the above figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates. The function $f(x, y, z) = 1$ whenever *x*, *y* are different and 0 otherwise. In addition the 3 inputs *x*, *y*, *z* are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit?

(a) $x'y + xy'$ (b) $x + y'z$

(c) $x'y'z' + xy'z$ (d) $xy + y'z + z'$

[GATE-2007]

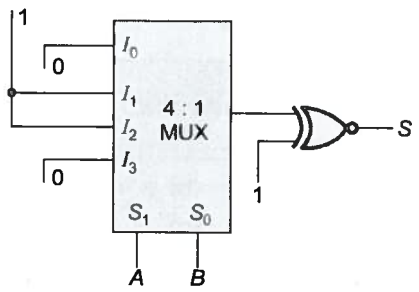
T19. A logic circuit has 3 inputs *A*, *B*, *C* and one output *Y*. The output is logic 1 when majority number of inputs are at logic 1. Find minimized expression for output *Y*.

■■■■

3 Combinational Logic Circuits

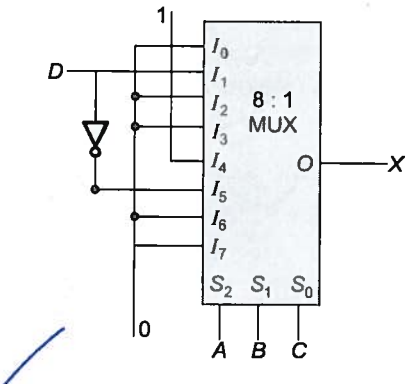
Multiple Choice Questions

Q.1 The circuit shown below does not represent



(a) $S(A, B) = \Sigma(1, 2)$
(b) EXOR gate with A and B as inputs
(c) $S(A, B) = \Pi(0, 3)$
(d) Equality function

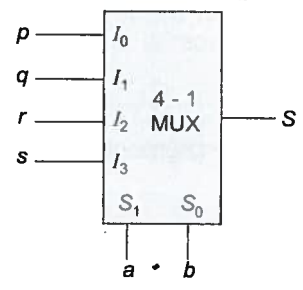
Q.2 The circuit below represents function $X(A, B, C, D)$ as:



(a) $\Sigma(3, 8, 9, 10)$
(b) $\Sigma(3, 8, 10, 14)$
(c) $\Pi(0, 1, 2, 4, 5, 6, 7, 11, 12, 13, 15)$
(d) $\Pi(0, 1, 2, 4, 5, 6, 7, 10, 12, 13, 15)$

Q.3 If half adders and full adders are implemented using gates, then for the addition of two 17 bit numbers (using minimum gates) the number of half adders and full adders required will be
(a) 0, 17 (b) 16, 1
(c) 1, 16 (d) 8, 8

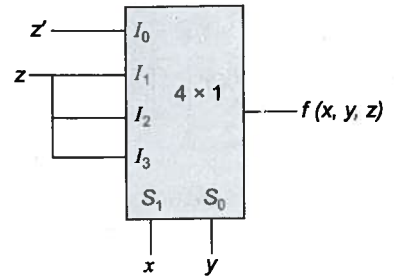
Q.4 Consider the function $F(a, b, c) = \bar{b}\,\bar{c} + bc + a\bar{b}$. If you implement F by means of 4-to-1 multiplexer then what will be the values of p, q, r, s, in the following figure.



(a) $\bar{C}$, C, 1, C
(b) C, $\bar{C}$, C, 0
(c) 1, 0, C, $\bar{C}$,
(d) C, $\bar{C}$, 1, $\bar{C}$

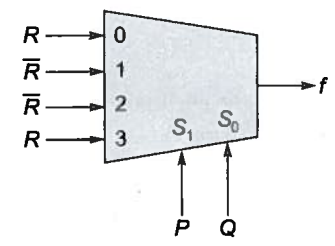
Q.5 x and y are two n-bit numbers. These numbers are added by a n-bit carry-lookahed adder, which uses k logic-levels. If the average gate delay of carry-lookahead adder is d then what will be the maximum delay of carry-lookahead adder circuit?
(a) n^2 (b) kd
(c) nkd (d) nd

Q.6 Consider the following circuit



If f (x, y, z) is $\Sigma(0, 3, 5, 7)$ then what will be the value of at I_0 and I_2 (respectively)?
(a) $\bar{Z}, Z$ (b) $\bar{Z}, \bar{Z}$
(c) Z, Z (d) $Z, \bar{Z}$

Q.7 The Boolean expression for the output f of the multiplexer shown below is



(a) $\overline{P \oplus Q \oplus R}$ (b) $P \oplus Q \oplus R$
(c) $P + Q + R$ (d) $\overline{P + Q + R}$

[GATE-2010]

Q.8 In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs, A_i and B_i are given by

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit S_i and carry bit C_{i+1} of the look-ahead carry adder are given by $S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i C_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively
(a) 6, 3 (b) 10, 4
(c) 6, 4 (d) 10, 5

Q.9 Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?
(a) 2^n line to 1 line
(b) 2^{n+1} line to 1 line
(c) 2^{n-1} line to 1 line
(d) 2^{n-2} line to 1 line [GATE-2007]

Q.10 Consider two 4-bit numers $A = A_3 A_2 A_1 A_0$ and $B = B_3 B_2 B_1 B_0$ and the expression $x_i = A_i B_i + \bar{A}_i \bar{B}_i$ for $i = 0, 1, 2, 3$. The expression

$$A_3\overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$$

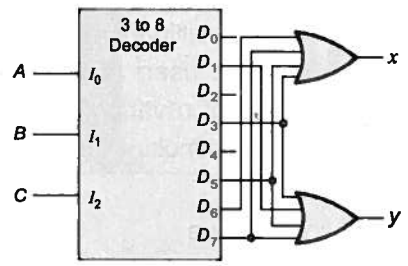
evaluates to 1 if
(a) $A = B$ (b) $A \neq B$
(c) $A > B$ (d) $A < B$
[DRDO-2009]

Q.11 Consider the multiplexer with X and Y as data inputs and Z as control input. $Z = 0$ selects input X and $Z = 1$ selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?
(a) R to X, 1 to Y, T to Z
(b) T to X, R to Y, T to Z
(c) T to X, R to Y, 0 to Z
(d) R to X, 0 to Y, T to Z [ESE-2009]

Q.12 Consider the following statements:
A multiplexer
1. selects one of the several inputs and transmits it to a single output
2. routes the data from a single input to one of many output
3. converts parallel data into serial data
4. is a combinational circuit

Which of these statements are correct?
(a) 1, 2 and 4 (b) 2, 3, and 4
(c) 1, 3 and 4 (d) 1, 2 and 3
[ESE-2000]

Q.13 The builiding block shown in figure is a active high output decoder

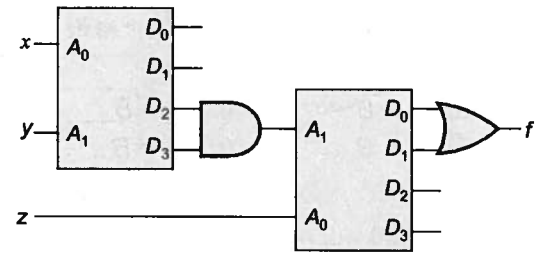


The output X is

(a) $AB + BC + CA$ (b) $A + B + C$

(c) ABC (d) None of these

Q.14 A logic circuit consist of two 2 ×4 decoders as shown in the figure. The output of decoder are as follow:



$D_0 = 1$ when $A_0 = 0, A_1 = 0$

$D_1 = 1$ when $A_0 = 1, A_1 = 0$

$D_2 = 1$ when $A_0 = 0, A_1 = 1$

$D_3 = 1$ when $A_0 = 1, A_1 = 1$

The value of $f(x, y, z)$ is

(a) 0 (b) z

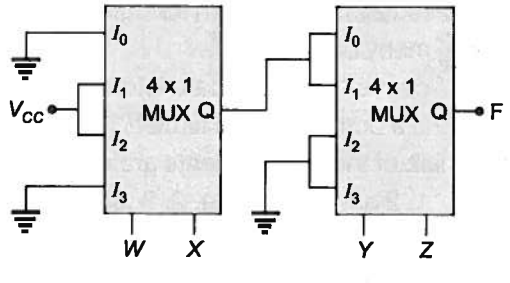
(c) $\bar{z}$ (d) 1

Q.15 Minimum number of NOR gates required to implement Sum in half-adder circuit is:

(a) 2 (b) 3

(c) 4 (d) 5

Q.16 In the circuit shown, W and Y are MSBs of the control inputs. The output is given by



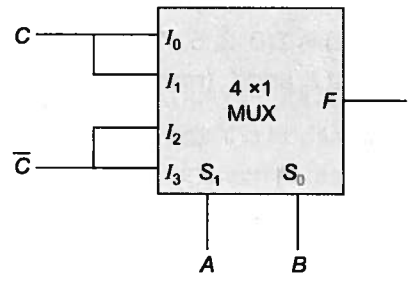
(a) $F = W\bar{X} + \bar{W}X + \bar{Y}\bar{Z}$

(b) $F = W\bar{X} + \bar{W}X + \bar{Y}Z$

(c) $F = W\bar{X}\bar{Y} + \bar{W}X\bar{Y}$

(d) $F = (\bar{W} + \bar{X})\bar{Y}\bar{Z}$

Q.17 The logic circuit realized by the circuit shown in the given figure will be

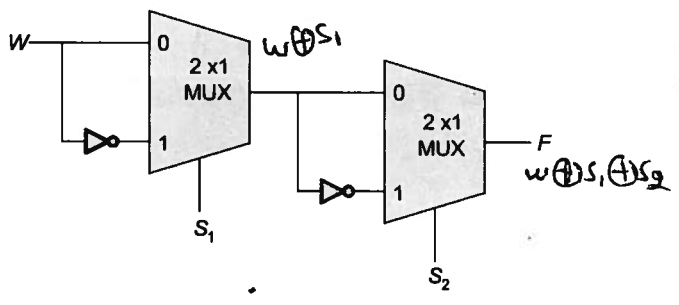


(a) $B \odot C$ (b) $F = B \oplus C$

(c) $A \odot C$ (d) $F = A \oplus C$

[ESE-1999]

Q.18 Consider the multiplexer based logic circuit shown in the figure.



Which one of the following Boolean functions is realized by the circuit?

(a) $F = W\bar{S}_1\bar{S}_2$

(b) $F = WS_1 + WS_2 + S_1S_2$

(c) $F = \bar{W} + S_1 + S_2$

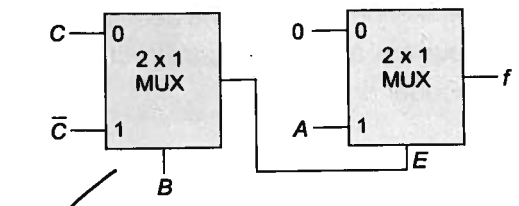
(d) $F = W \oplus S_1 \oplus S_2$ **[GATE-2014]**

Q.19 The minimum number of 2 × 1 multiplexers required to implement a half adder circuit are [when only basic inputs are available, compliments are not available].

(a) 4 (b) 2

(c) 3 (d) 5

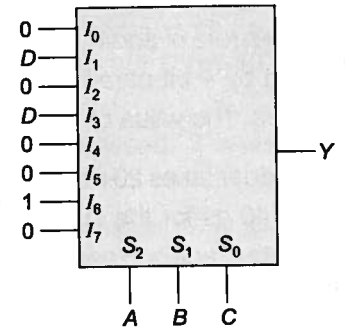
Q.20 The Boolean function 'f' implemented as shown in the figure using two input multiplexers is



(a) $A\bar{B}C + AB\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$

(c) $\bar{A}BC + AB\bar{C}$ (d) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

Q.21 An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. The output

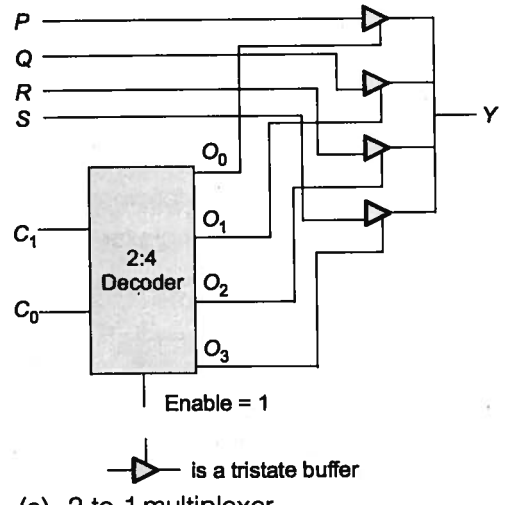


(a) $Y = A\bar{B}C + A\bar{C}D$ (b) $Y = \bar{A}BC + A\bar{B}D$

(c) $Y = AB\bar{C} + \bar{A}CD$ (d) $Y = \bar{A}\bar{B}D + A\bar{B}C$

[GATE-2014]

Q.22 The functionality implemented by the circuit below is



(a) 2-to-1 multiplexer

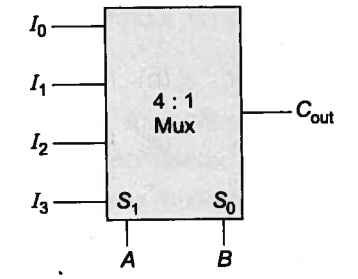
(b) 4-to-1 multiplexer

(c) 7-to-1 multiplexer

(d) 6-to-1 multiplexer

[GATE-2016]

Q.23 A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry and C_{out} is the output carry. A and B are to be used as the select bits with A being the more significant select bit.



Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0, I_1, I_2 and I_3 so that the output is C_{out}?

(a) $I_0 = 0, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$

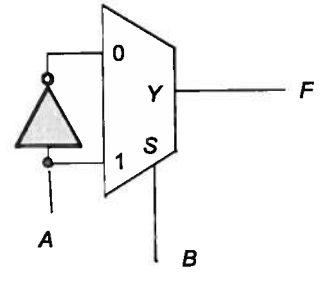
(b) $I_0 = 1, I_1 = C_{in}, I_2 = C_{in}$ and $I_3 = 1$

(c) $I_0 = C_{in}, I_1 = 0, I_2 = 1$ and $I_3 = C_{in}$

(d) $I_0 = 0, I_1 = C_{in}, I_2 = 1$ and $I_3 = C_{in}$

[GATE-2016]

Q.24 Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is?

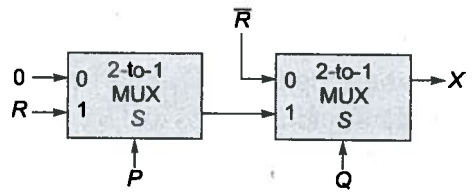


(a) $A \oplus B$ (b) $\overline{A+B}$

(c) $A + B$ (d) $\overline{A \oplus B}$

[GATE-2016]

Q.25 Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



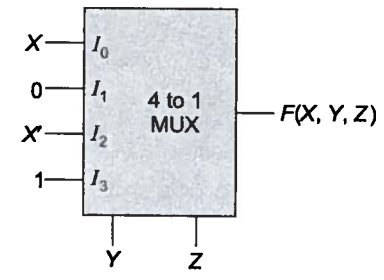
The minimal sum of products form of the output X is

(a) $\bar{P}\bar{Q}+PQR$ (b) $\bar{P}Q+QR$

(c) $PQ+\bar{P}\bar{Q}\bar{R}$ (d) $\bar{R}\bar{Q}+PQR$

[GATE-2016]

Q.26 A 4 to 1 multiplexer to realize a Boolean function $F(X, Y, Z)$ is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for $F(X, Y, Z)$ is



(a) $\Sigma m(2, 3, 4, 7)$ (b) $\Sigma m(1, 3, 5, 7)$

(c) $\Sigma m(0, 2, 4, 6$ (d) $\Sigma m(2, 3, 5, 6)$

[GATE-2016]

Numerical Data Type Questions

Q.27 Minimum number of NAND gates required to implement Sum in half-adder circuit is ____.

Q.28 Minimum number of 2 × 1 multiplexers required to realize the following function is ____.

$$f(A,B,C) = \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

(Assume that inputs are available only in true form and Boolean constants 1 and 0 are available.)

Q.29 The number of 2-to-4-line decodes with enable input are needed to construct a 4-to-16-line decoder are ____.

[DRDO-2009]

Q.30 A person wants to design a 4 × 1 multiplexer using only NAND gates. If NAND gates with any number of inputs are available, then total number of NAND gates required are ____.

Q.31 A one bit full adder takes 75 nsec to produce sum and 50 nsec to produce carry. A 4 bit parallel adder is designed using this type of full adder. The maximum rate of additions per second can be provided by 4 bit parallel adder is $A \times 10^6$ additions/sec. The value of A is ____.

Q.32 A 1 bit full adder takes 20 ns to generate carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second, when four 1 bit full address are cascade?

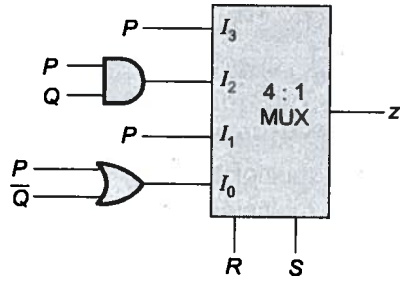
[ESE-2005]

Try Yourself

T1. Design a logic circuit for detecting equality of 2-bit binary numbers.

T2. Design a combination circuit that accepts a 2 bit number as input and generate binary number equal to square of the input number.

T3. For the circuit shown in the following figure, $I_0 - I_3$ are inputs to the 4 : 1 multiplexer. R (MSB) and S are control bits.



The output Z can be represented by

(a) $PQ+P\bar{Q}S+\bar{Q}\bar{R}\bar{S}$

(b) $P\bar{Q}+PQ\bar{R}+\bar{P}\bar{Q}\bar{S}$

(c) $P\bar{Q}\bar{R}+\bar{P}QR+PQRS+\bar{Q}\bar{R}\bar{S}$

(d) $PQ\bar{R}+PQR\bar{S}+P\bar{Q}\bar{R}S+\bar{Q}\bar{R}\bar{S}$

[GATE-2008]

Statement for Linked Answer Question (4 and 5):
Two products are sold from a vending machine, which has two push buttons P_1 and P_2. When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

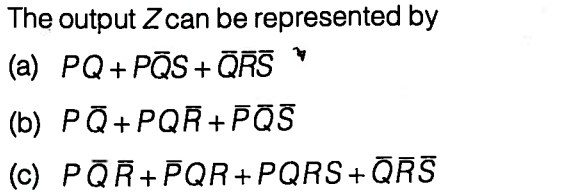
If no buttons are pressed, '0' is displayed, signifying 'Rs. 0'

If only P_1 is pressed, '2' is displayed, signifying 'Rs.2'

If only P_2 is pressed, '5' is displayed, signifying 'Rs.5'

If both P_1 and P_2 are pressed, 'E' is displayed, signifying 'Error'

The names of the segments in the 7-segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.



Consider:

(i) push button pressed/not pressed in equivalent to logic 1/0 respectively,

(ii) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively

T4. If segments a to g are considered as functions of P_1 and P_2, then which of the following is correct?

(a) $g = \bar{P}_1 + P_2, d = c + e$

(b) $g = P_1 + P_2, d = c + e$

(c) $g = \bar{P}_1 + P_2, e = b + c$

(d) $g = P_1 + P_2, e = b + c$

T5. What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of the driver for this 7-segment display?

(a) 3 NOT and 4 OR

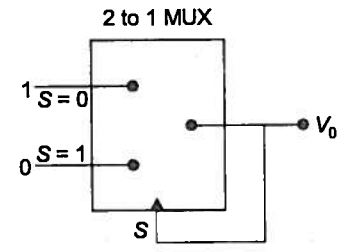
(b) 2 NOT and 4 OR

(c) 1 NOT and 3 OR

(d) 2 NOT and 3 OR

T6. The number of 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates are ____.

T7. A 2-to-1 digital multiplexer having a switching delay of 1 μs is connected as shown in the figure. The output of the multiplexer is tied to its own select input S. The input which gets selected when $S = 0$ is tied to 1 and the input that gets selected when $S = 1$ is tied to 0. The output V_0 will be



(a) 0

(b) 1

(c) Pulse train of frequency 0.5 MHz

(d) Pulse train of frequency 1.0 MHz

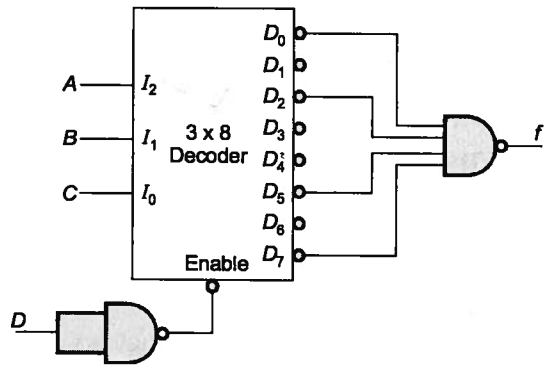
T8. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the dealy of each gate is1 time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

(a) 4 time units (b) 6 times units

(c) 10 times units (d) 12 times units

[GATE-2004]

T9. The logic function $f(A, B, C, D)$ implemented by the circuit shown below is



(a) $\bar{D}(A \oplus C)$ (b) $D(A \odot C)$

(c) $\bar{D}(A \oplus B)$ (d) $D(A \odot B)$

T10. Without any additional circuitry, an 8 :1 MUX can be used to obtain

(a) some but not all Boolean functions of 3 variables

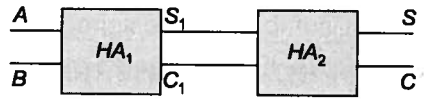
(b) all functions of 3 variables but none of 4 variables

(c) all functions of 3 variables and some but not all of 4 variables

(d) all functions of 4 variables

[GATE-EC:2003]

T11. Two Half Adders are connected in cascade as shown in figure below. The output "S" and "C" are



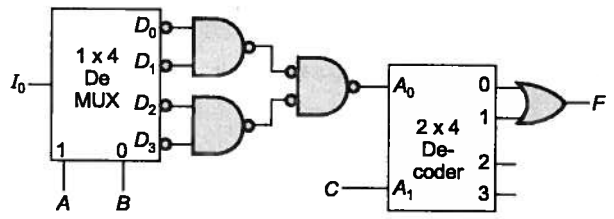
(a) $S = A \oplus B,\ C = AB$

(b) $S = A \odot B, C = 0$

(c) $S = A + B,\ C = 0$

(d) $S = AB,\ C = 0$

T12. Consider the logic circuit given below



The minimized expression for F is

(a) $\bar{C}$ (b) I_0

(c) C (d) $\bar{I}_0$

T13. A 4 bit binary adder is adding two *BCD* numbers and producing the sum output $S_3S_2S_1S_0$ along with the carry output C_0. It is required to design a checking circuit such that the checking circuit output must be zero, whenever the binary adder output is invalid *BCD*, the boolean expression of checking circuit is

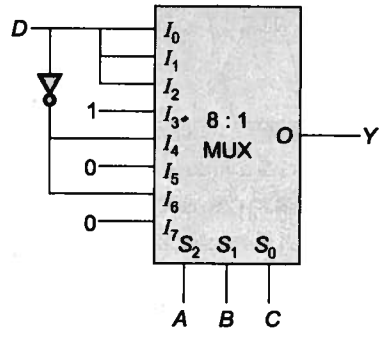
(a) $\bar{C}_0\bar{S}_3 + \bar{C}_0\bar{S}_2\bar{S}_1$

(b) $C_0 + S_3S_2 + S_2S_1$

(c) $(\bar{C}_0 + \bar{S}_3)\cdot(\bar{C}_0 + \bar{S}_2 + \bar{S}_1)$

(d) None of the above

T14. For the given multiplexer, Y is equal to



(a) $A\bar{C}\bar{D} + \bar{A}BC + \bar{A}D$

(b) $A\bar{B}\bar{C} + A\bar{C}\bar{D} + \bar{A}D$

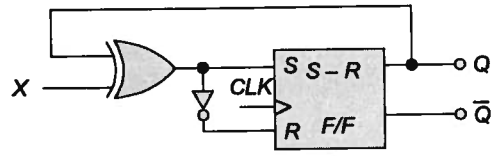
(c) $\bar{A}\bar{B}\bar{C} + AC\bar{D} + \bar{A}\bar{D}$

(d) $A\bar{C}\bar{D} + \bar{A}\bar{B}D + A\bar{D}$

4 Sequential Circuits

Multiple Choice Questions

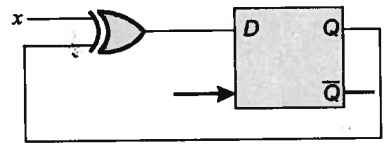
Q.1 Identify the type of the flip-flop



(a) R-S flip-flop (b) J-K flip-flop

(c) D flip-flop (d) T-flip-flop

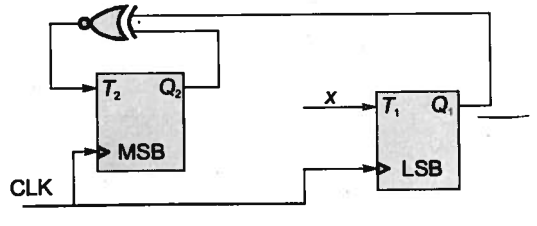
Q.2 The circuit acts as



(a) D-Flip Flop (b) T-Flip Flop

(c) Both A and B (d) None

Q.3 Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below



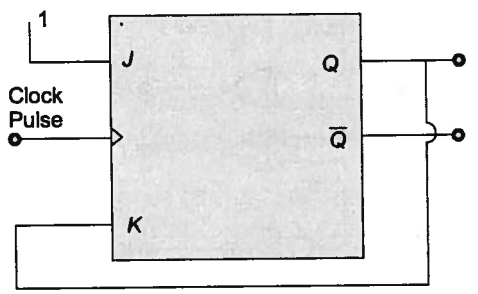
To complete the circuit, the input X should be

(a) Q_2' (b) $Q_2 + Q_1$

(c) $(Q_1 \oplus Q_2)'$ (d) $Q_1 \oplus Q_2$

[GATE-2004]

Q.4 In figure, assume that initially $Q = 1$. With clock pulses being given, the subsequent states of Q will be



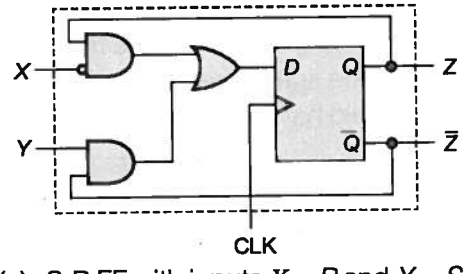
(a) 1, 0, 1, 0, 1, 0, 1

(b) 0, 0, 1, 0, 0, 1, 0....

(c) 1, 1, 0, 1,1, 0,1

(d) 0,1, 0, 1, 0, 1, 0....

Q.5 A sequential circuit using D flip-flop and logic gates is shown in figure where X and Y are the inputs and Z is the output. The circuit is



(a) S-R FF with inputs $X = R$ and $Y = S$

(b) S-R FF with inputs $X = S$ and $Y = R$

(c) J-K FF with inputs $X = J$ and $Y = K$

(d) J-K FF with inputs $X = K$ and $Y = J$

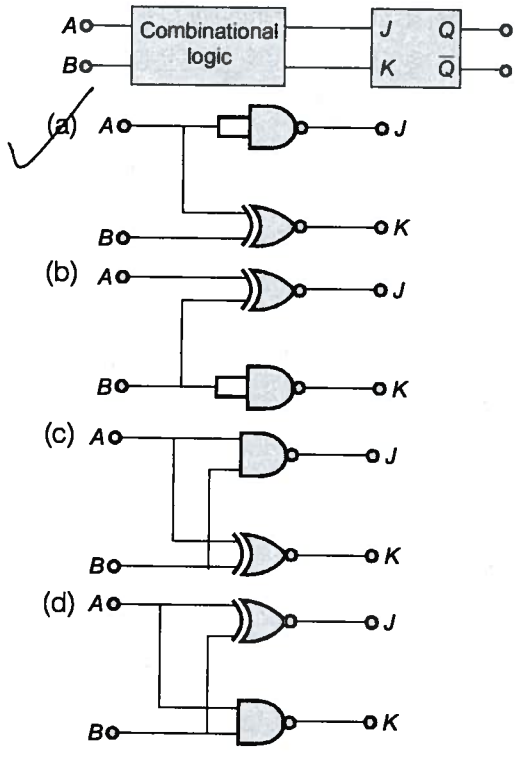
Q.6 The characteristic equation of the T-FF is given by

(a) $Q^+ = T\bar{Q} + Q\bar{T}$ (b) $Q^+ = \bar{T}Q + TQ$

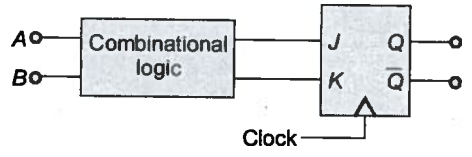
(c) $Q^+ = TQ$ (d) $Q^+ = T\bar{Q}$

Q.7 The circuit realization of the combination logic block shown in figure to obtain the following truth table will be,

A	B	Q_{n+1}
0	0	$\overline{Q}_n$
0	1	1
1	0	Q_n
1	1	0



Q.8 To realize the given truth table from the circuit shown in the figure, the input to J in terms of A and B would have to be



Truth Table

A	B	Q_{n+1}
0	0	Q_n
0	1	1
1	0	Q_n
1	1	0

(a) $\overline{A}$ (b) B
(c) $\overline{A}\overline{B}$ (d) $\overline{A}B$

Q.9 X-Y flip flop, whose Characteristic Table is given below is to be implement using a J-K flip flop

X	Y	Q_{n+1}
0	0	1
0	1	$\overline{Q_n}$
1	0	Q_n
1	1	0

This can be done by making
(a) $J=\overline{Y}, K=X$ (b) $J=\overline{X}, K=Y$
(c) $J=Y, K=\overline{X}$ (d) $J=X, K=\overline{Y}$

Q.10 Match **List-I** with **List-II** and select the correct answer using the codes given below the lists:

List-I
A. Shift register
B. Counter
C. Decoder

List-II
1. Frequency division
2. Addressing in memory chips
3. Serial to parallel data conversion

Codes:

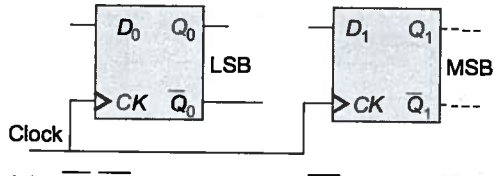
	A	B	C
(a)	3	2	1
(b)	1	2	2
(c)	2	1	3
(d)	3	1	2

[EC : GATE-2004]

Q.11 Two D-flip flops, as shown below are to be connected as a synchronous counter that goes through the following $Q_1\ Q_0$ sequence

$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00...$

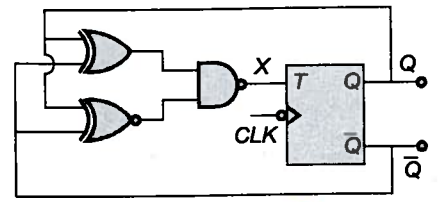
The inputs D_0 and D_1 respectively should be connected as



(a) $\overline{Q_1}\ \overline{Q_0}$ and $Q_1\ Q_0$ (b) $\overline{Q_0}$ and Q_1
(c) $\overline{Q_1}Q_0$ and $\overline{Q_1}\ Q_0$ (d) $\overline{Q_1}$ and Q_0

[EC : GATE-2006]

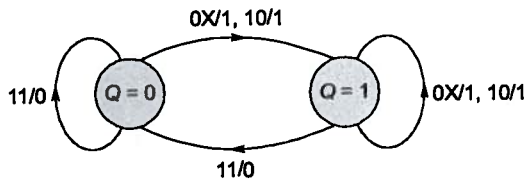
Q.12 The clock frequency applied to the digital circuit shown in figure below is 1 kHz. If the initial state of the output Q of the flip-flop is '0', then the frequency of the output waveform Q in kHz is



(a) 0.25 (b) 0.5
(c) 1 (d) 2

[GATE-2013]

Q.13 A state diagram of a logic which exhibits a delay in the output is shown in the figure, where X is the do not care condition, and Q is the output representing the state.

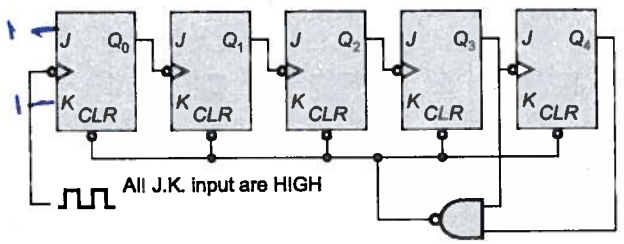


The logic gate represented by the state diagram is
(a) XOR (b) OR
(c) AND (d) NAND **[GATE-2014]**

Q.14 Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
(a) Asynchronous operation
(b) Low input voltage
(c) Gate impedance
(d) Cross coupling **[ESE-2013]**

Q.15 Synchronous counters eliminate the delay problems encountered with asynchronous (ripple) counter because the
(a) input clock pulses are applied only to the first and the last stages
(b) input clock pulses are applied only to the last stage
(c) input clock pulses are not used to activate any of the counter stages
(d) input clock pulses are applied simultaneously **[ESE-2013]**

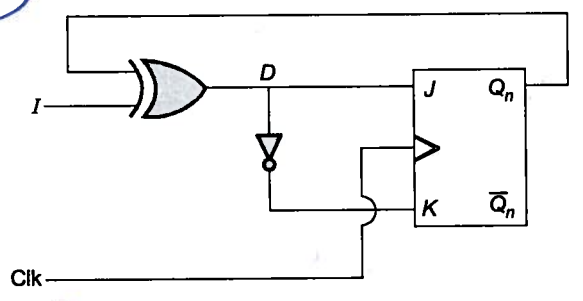
Q.16 The mod-number of the asynchronous counter shown in figure



(a) 24 (b) 48
(c) 25 (d) 36

Q.17 The output of moore sequential machine is a function of
(a) all present states of machine
(b) all inputs
(c) all combination of inputs and present state
(d) few combination of inputs and present state

Q.18 If I is set high is circuit given below then Q_{n+1} is



(a) complementary (b) Q_n
(c) high (d) low

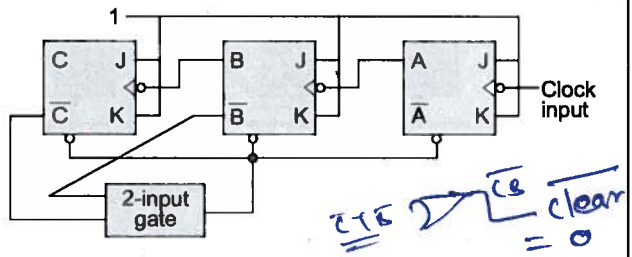
Q.19 The number of unused states in a 4-bit Johnson counter is
(a) 2 (b) 4
(c) 8 (d) 12

[ESE-2003]

Q.20 A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then
(a) R = 10 ns, S = 40 ns
(b) R = 40 ns, S = 10 ns
(c) R = 10 ns, S = 30 ns
(d) R = 30 ns, S = 10 ns

[GATE-2003]

Q.21 In the modulo-6 ripple counter shown in the figure, the output of the 2-input gate is used to clear the *J-K* flip-flops.

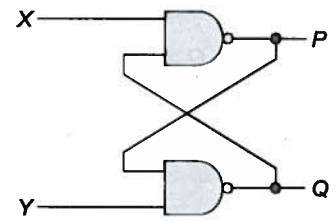


The 2-input gate is

(a) a NAND gate (b) a NOR gate
(c) an OR gate (d) an AND gate

[GATE-2004]

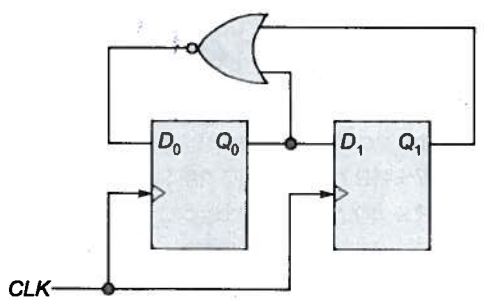
Q.22 The following binary values were applied to the *X* and *Y* inputs of the NAND latch shown in the figure in the sequence indicated below:
$X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1.$
The corresponding stable P, Q outputs will be



(a) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$
(b) $P = 1, Q = 0; P = 0, Q = 1$ or $P = 0, Q = 1; P = 0, Q = 1$
(c) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$ or $P = 0, Q = 1$
(d) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$

[GATE-2007]

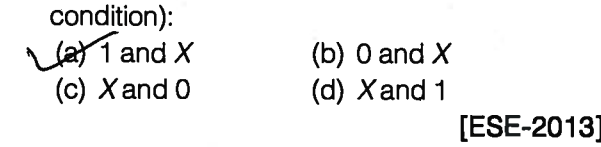
Q.23 For the circuit shown, the counter state $(Q_1 Q_0)$ follows the sequence



(a) 00, 01, 10, 11, 00 ...
(b) 00, 01, 10, 00, 01 ...
(c) 00, 01, 11, 00, 01 ...
(d) 00, 10, 11, 00, 10 ...

[GATE-2007]

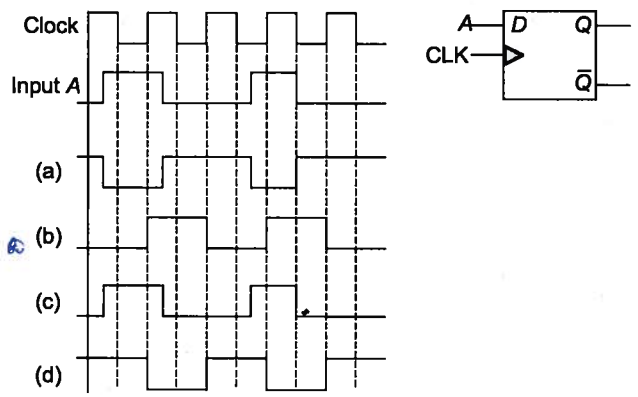
Q.24 The figure below shows a 3-bit ripple counter, with Q_2 as the MSB. The flip-flop are rising-edge triggered. The counting direction is



(a) always down
(b) always up
(c) up or down depending on the initial state of Q_0 only
(d) up or down depending on the initial states of Q_2, Q_1 and Q_0

[GATE-IN:2009]

Q.25 The input *A* and clock applied to the *D* flip-flop are shown in figure below. The output *Q* is,



Q.26 The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n a K_n are respectively (*X* represents don't care condition):

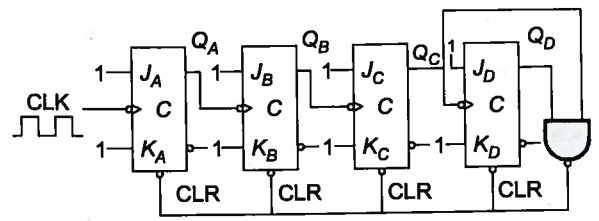
(a) 1 and *X* (b) 0 and *X*
(c) *X* and 0 (d) *X* and 1

[ESE-2013]

Q.27 The Q-output of J-K flip-flop is '1'. The output does not change when a clock-pulse is applied. The input J and K will be respectively (x-don't care state)

(a) 0 and x (b) 0 and 1
(c) 1 and 0 (d) x and 0

Common Data for Questions (28 and 29):
A counter is shown below:



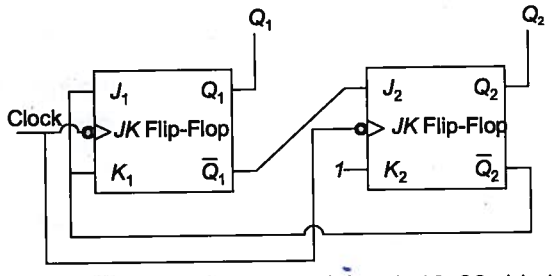
Q.28 The counter shown is

(a) Mod-12 (b) Mod-9
(c) Mod-14 (d) None of these

Q.29 Frequency of output Q_D for 1 MHz clock is

(a) 63.3 kHz (b) 83.3 kHZ
(c) 73.3 kHz (d) None of these

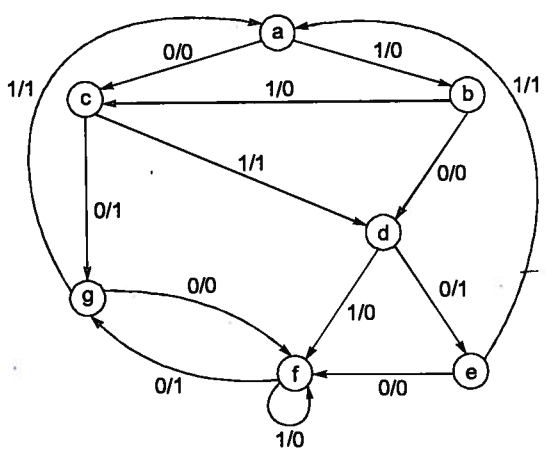
Q.30 What are the counting states (Q_1, Q_2) for the counter shown in the figure below?



(a) 01, 10, 11, 00, 01... (b) 11, 10, 00, 11, 10...
(c) 00, 11, 01, 10, 00... (d) 01, 10, 00, 01, 10...

[EC GATE-2009]

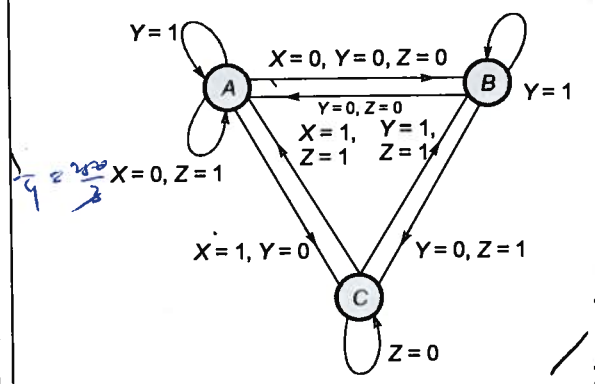
Q.31 Following state diagram shows clocked sequential circuit:



How many minimum number of states the sequential circuit has?

(a) 6 (b) 7
(c) 5 (d) 4

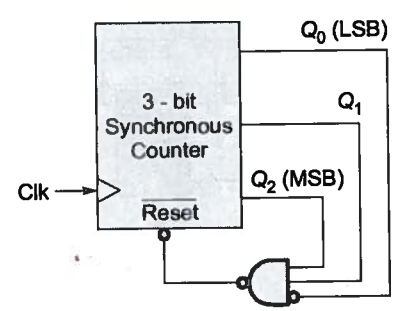
Q.32 The state transition diagram for a finite state machine with states *A*, *B* and *C*, and binary inputs *X*, *Y* and *Z*, is shown in the figure.
Which one of the following statements is correct?



(a) Transitions from State *A* are ambiguously defined.
(b) Transitions from State *B* are ambiguously defined.
(c) Transitions from State *C* are ambiguously defined.
(d) All of the state transitions are defined unambiguously.

[GATE-2016]

Q.33 For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero.

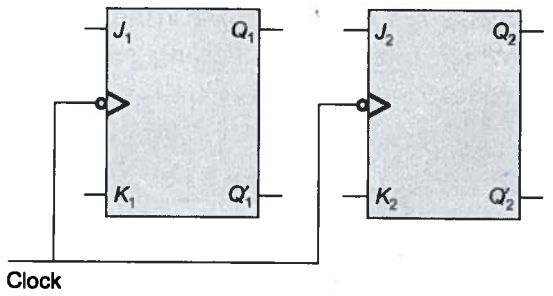


If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

(a) mod-5 counter (b) mod-6 counter
(c) mod-7 counter (d) mod-8 counter

[GATE-2016]

Q.34 A synchronous counter using two J - K flip flops that goes through the sequence of states: $Q_1Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00$ ... is required. To achieve this, the inputs to the flip flops are:



(a) $J_1 = Q_2, K_1 = 0 ; J_2 = Q_1', K_2 = Q_1$

(b) $J_1 = 1, K_1 = 1 ; J_2 = Q_1, K_2 = Q_1$

(c) $J_1 = Q_2, K_1 = Q_2' ; J_2 = 1, K_2 = 1$

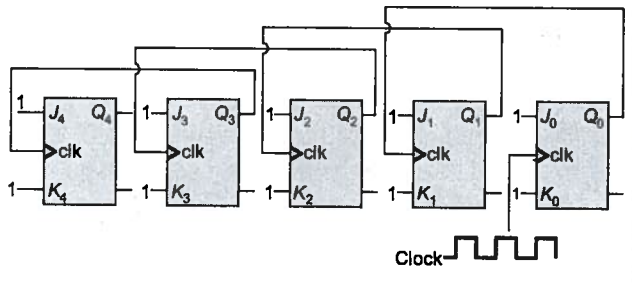
(d) $J_1 = Q_2', K_1 = Q_2, J_2 = Q_1, K_2 = Q_1'$

[GATE-2016]

Numerical Data Type Questions

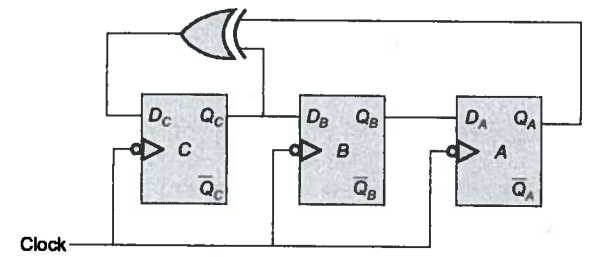
Q.35 The minimum number of flip-flops required by a module-8 counter is 3.

Q.36 Five JK flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is 62.5 KHz.

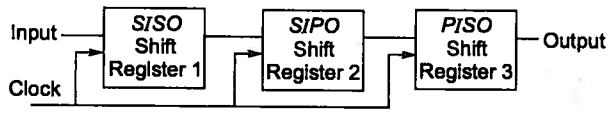


[GATE-2014]

Q.37 A digital circuit is designed with three *D*-flip flops and an Ex-OR gate as shown in below figure. If the initial value of $Q_A\ Q_B\ Q_C$ was 110 then the minimum number of clock pulses required to get $Q_A\ Q_B\ Q_C$ as 011 is _____.



Q.38 Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with a common clock pulse.



A 4 bit data 1011 is applied to the shift register 1.The minimum number of clockpulses required to get same input data at output with same clock are_____.

Common Data for Questions (39 and 40):

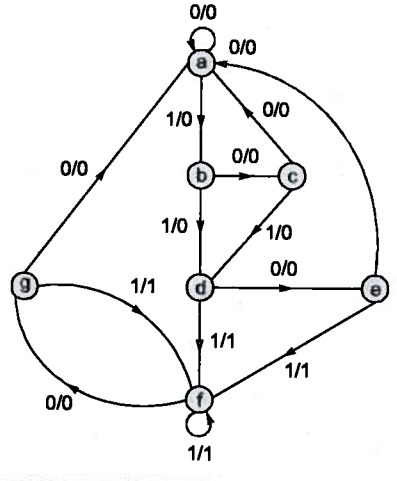
A Mealy system produces a 1 output if the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's.

Q.39 The minimum number of states for this system is _____.

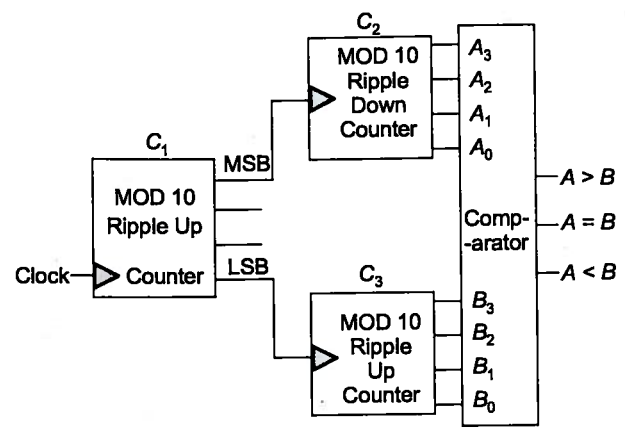
Q.40 The flip-flops required to implement this system are _____.

Try Yourself

T1. Reduce the following state diagram and also write the reduced state table.



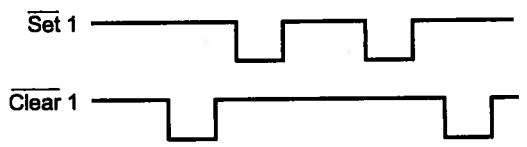
T2. Consider the circuit given below:



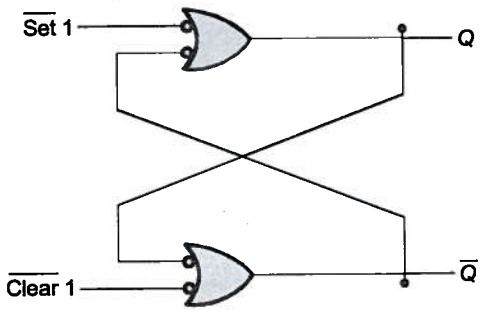
MSB and LSB of MOD 10 ripple up counter acts as clock to 4 bit ripple down and up counter respectively. Initially all the counter were cleared and output of comparator was $A = B$. The clock pulse is applied. Find the minimum number of clock pulses required to make $A = B$ again.

[Ans: 17]

T3. The waveforms.



are applied to the inputs of the latch



Draw the waveform at Q and explain.

[ESE-2006]

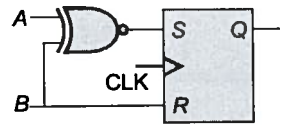
T4. Using J-K flip-flop, design a counter which has the following count sequence:

0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

Draw the excitation table, logic diagram and state diagram.

[ESE-2007]

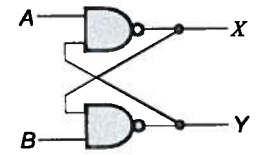
T5. An AB flip-flop is constructed from an SR flip-flop as shown in fig. The expression for next state Q^+ is



(a) $\bar{A}\bar{B} + AQ$ (b) $\bar{A}\bar{B} + \bar{B}Q$

(c) Both A and B (d) None of the above

T6. In figure initially $A = 1$ and $B = 1$, the input B is now replaced by a sequence 1 0 1 0 1 0 ... the outputs X and Y will be



(a) Fixed at 0 and 1 respectively

(b) Fixed at 1 and 0, respectively

(c) $X = 1\ 0\ 1\ 0$ ... while $Y = 1\ 0\ 1\ 0$ ...

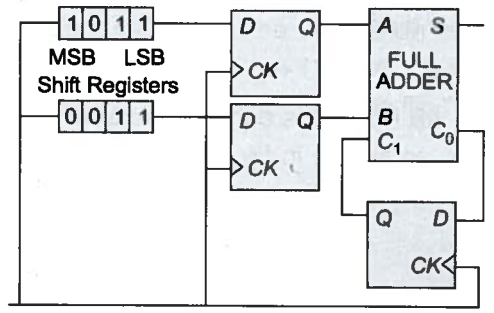
(d) $X = 1\ 0\ 1\ 0$ ... while $Y = 0\ 1\ 0\ 1$ ...

T7. A new Flip-Flop is having behaviour as described below. It has two inputs X and Y and when both inputs are same and they are 1,1, the flip-flop is going to set else flip-flop resets. If both inputs are different and they are 0, 1, filp-flop complements itsself otherwise it is going to retain the last state. Which of the following expression is the characteristic expression for the new flip flop?

(a) $xQ + y\bar{Q}$ (b) $x\bar{Q} + yQ$

(c) $x\bar{Q} + y\bar{Q}$ (d) None

T8. For the circuit shown in the figure below, two 4-bit parallel-in-serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in the clear state. After applying two clock pulses, the outputs of the full adder should be



(a) $S = 0 \quad C_0 = 1$ (b) $S = 0 \quad C_0 = 0$
(c) $S = 1 \quad C_0 = 1$ (d) $S = 1 \quad C_0 = 0$

[EC GATE-2006]

T9. Design a MOD-10 synchronous counter using J-K flip-flops giving state diagram excitation table, K-maps and circuit diagram.

[ESE-2008]

T10. Design a mod-6 counter to go through the sequence of states as given in the table below using S-R flip-flop:

Sequence No.	Required State Sequence		
0	0	0	0
1	0	1	0
2	0	1	1
3	1	1	0
4	1	0	1
5	0	0	1

→ Repeat from 0 0 0

Show the state table indicating the present state, the next state for each present state along with the input requirements of each of the S and R inputs. Show clearly the minimization of logic requirements using K-maps. Write the logical expressions for each excitation input of all the flip-flops. Draw the logic diagram of the counter designed by you.

[ESE-2009]

T11. Using *T* flip-flop and logic gates, design a *L-M* edge triggered flip-flop having a truth table as given below:

L	M	Q_+
0	0	0
0	1	$\overline{Q}$
1	0	1
1	1	$\overline{Q}$

[ESE-2014]

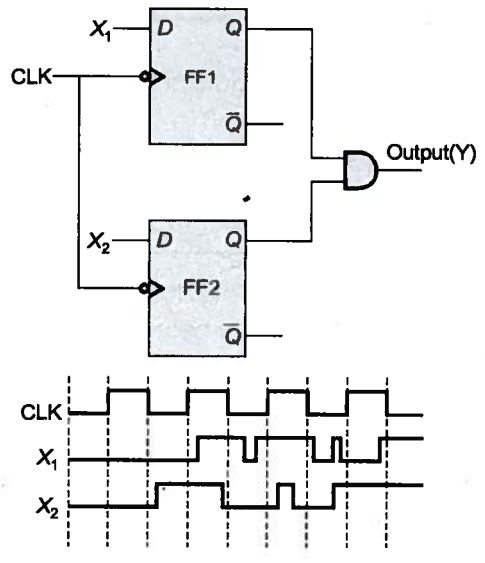
T12. Design a Synchronous BCD Counter using J-K Flip-flops.

T13. Design a counter using D flip-flop that goes through states, 0, 1, 2, 4, **0**. The undesired (unused) states must always go to zero (000) on the next clock pulse.

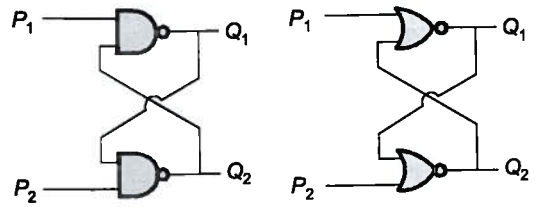
T14. Desigh synchronous counter for given count sequence
$00 \rightarrow 10 \rightarrow 01 \rightarrow 11$.

T15. Consider a mod-1000 ripple up counter. The duty cycle for its MSB is _____%.

T16. Consider the flip-flop circuit diagram shown below. Draw output waveform for the circuit.



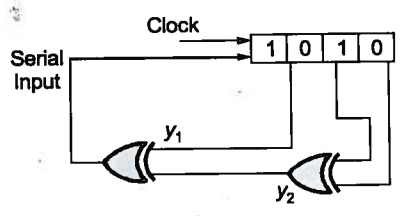
T17. Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then after a few second, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are



(a) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
(b) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)
(c) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)
(d) NAND: first (1, 0) then (1, 0) NOR: first (0, 1) then (0, 0)

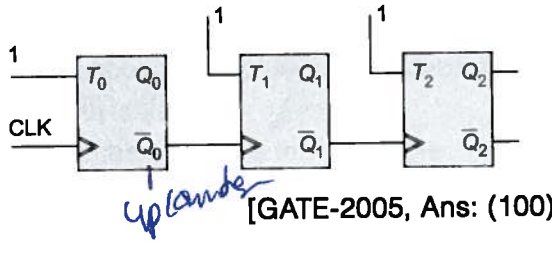
[EC : GATE-2009, Ans: (b)]

T18. The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again?



[Ans: (7)]

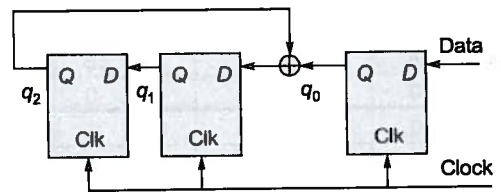
T19. The given figure shows a ripple counter using positive edge triggered flip-flops.
If the present state of the counter is $Q_2\ Q_1\ Q_0 = 011$, then its next state ($Q_2\ Q_1\ Q_0$) will be 100



up counter

[GATE-2005, Ans: (100)]

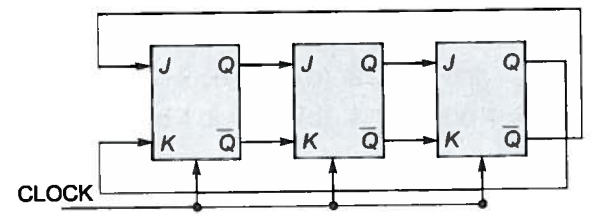
T20. Consider the circuit in the diagram. The ⊕ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data : 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2\ q_1\ q_0$ are
(a) 000 (b) 001
(c) 010 (d) 101

[GATE-2006, Ans: (c)]

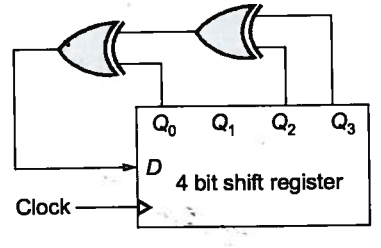
T21. For the initial state of 000, the function performed by the arrangement of the J-K flip flops in the figure



(a) Shift Register (b) Mod-3 counter
(c) Mod-6 counter (d) Mod-2 counter

[EC : GATE-1993]

T22. A 4 bit right shift, shift register is shifting the data to the right for every clock pulse The serial input *D* is derived by using Ex-OR gates as shown in the figure. After three clock pulses the content in the shift register is to be 1010 at $Q_0Q_1Q_2Q_3$, what will be the initial content of the register.



(a) 1100 (b) 1010
(c) 0011 (d) 0101

T23. Consider the following state transition table with two state variables A and B and the input variable x and the output variable y

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

If the initial state is $A = 0$ and B = 0, what is the minimum length of an input string which will take the macine to the state $A = 1$ and $B = 1$ with output $y = 1$?

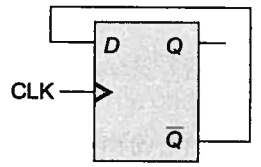
(a) 3 (b) 4
(c) 5 (d) 6

[DRDO-2009]

T24. If a counter having 10 FF's is initially at 0, what count will it hold after 2060 pulses?

(a) 000 000 1100 (b) 000 001 1100
(c) 000 001 1000 (d) 000 000 1110

T25. The frequency of the clock signal applied to the rising edge triggered D-flip flop shown in the following figure is 10 kHz. What is the output frequency at the flip flop output Q? (in kHz)



T26. How many pulses are needed to change the contents of a 8-bit up-counter from 10101100 to 00100111 (right most bit is the LSB)?

[IT GATE-2005]

■■■■

5 Semiconductor Memories

Multiple Choice Questions

Q.1 Which one of the following statements is correct?

(a) PROM contains a programmable 'AND' array and a fixed 'OR' array
(b) PLA contains a fixed 'AND' array and a programmable 'OR' array
(c) PROM contains a fixed 'AND' array and a programmable 'OR' array
(d) PLA contains a programmable 'AND' array and a programmable 'NOR' array

[ESE-2004]

Q.2 A ROM is to be used to implement a "squarer", which outputs the square of a 4-bit number. What must be the size of the ROM?

(a) 16 address lines and 16 data lines
(b) 4 address lines and 8 data lines
(c) 8 address lines and 8 data lines
(d) 4 address lines and 16 data lines

[ESE-2004]

Q.3 A single ROM is used to design a combinational circuit described by a truth table. What is the number of address lines in the ROM?

(a) Number of input variables in the truth table
(b) Number of output variables in the truth table
(c) Number of input plus output variables in the truth table
(d) Number of lines in the truth table

[ESE-2006]

Q.4 How may address inputs, data outputs are required for a 16k × 12 memory

(a) 12,12 (b) 16,12
(c) 14,12 (d) 16,16

Q.5 Consider the following statements for a DRAM:

1. Bit is stored as a charge.
2. It is made of MOS transistors.
3. Speed of DRAM is faster than processors.
4. Each memory cell requires six transistors.

Which of these statements are correct?

(a) 1 and 2 only (b) 2 and 3 only
(c) 3 and 4 only (d) 1, 2, 3 and 4

Numerical Data Type Questions

Q.6 A semiconductor RAM has a 12 bit address register and an 8 bit data register. The total number of bits in the memory is _____.

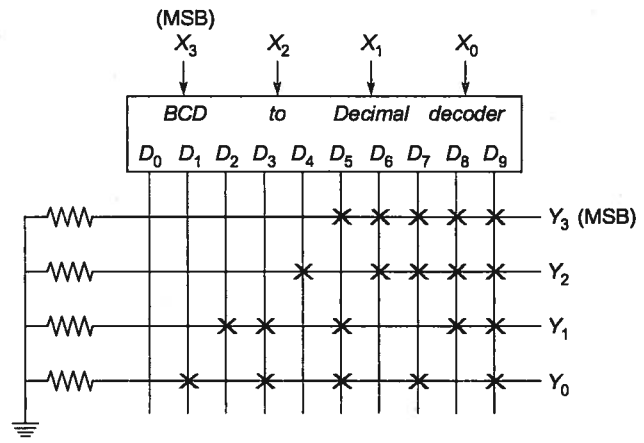
Q.7 It is desired to have 64 × 8 memory and if only 16 × 4 size chips are available then number of chips required are _____.

Q.8 The minimum number of MOS transistors required to make a dynamic RAM cell are _____.

Q.9 The minimum number of MOS transistors required to make a static RAM cell are _____.

Try Yourself

T1. Consider the ROM shown below.



If the coding scheme for $X_3 X_2 X_1 X_0$ is BCD then find coding scheme for $Y_3 Y_2 Y_1 Y_0$.

T2. Impliment the following logical expression using ROM circuit.

$Y_3 (A, B, C) = \Sigma m(1, 2, 4, 7)$
$Y_2 (A, B, C) = \Sigma m(1, 3, 5, 6)$
$Y_1 (A, B, C) = \Sigma m(0, 2, 3, 4, 7)$
$Y_0 (A, B, C) = \Sigma m(3, 5, 6, 7)$

T3. Implement BCD to excess - 3 convertor.

■■■■

6 Integrated-Circuit Logic Families

Multiple Choice Questions

Q.1 Consider the following statements describing the property of a complementary MOS (CMOS) inverter:

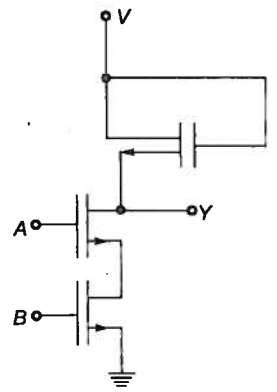
1. It is a combination of an n-channel FET and a p-channel FET.
2. There is power dissipation when the input carries the logical 1 signal.
3. There is no power dissipation when the input carries the logical 1 signal.
4. There is power dissipation during transition from 0 to 1 or from 1 to 0.

Which of the statements given above are correct?

(a) 1, 2 and 3 (b) 2, 3 and 4
(c) 1, 3 and 4 (d) 1, 2 and 4

[ESE-2006]

Q.2 The NMOS circuit shown below is a gate of the type



(a) NAND (b) NOR
(c) AND (d) EXCLUSIVE - OR

[ESE-2003(EE)]

Q.3 A inverter gate has guaranteed output levels as: logic '1' = 3.8 V and logic '0' = 0.7 V. The maximum low level input voltage at which the output remains high = 2 V. The minimum high-level input voltage at which the output remains low = 3.1 V. What are the noise margins of this gate?

(a) $NM_H = 2.4$ V, $NM_L = 1.8$ V
(b) $NM_H = 1.8$ V, $NM_L = 1.3$ V
(c) $NM_H = 0.7$ V, $NM_L = 1.8$ V
(d) $NM_H = 0.7$ V, $NM_L = 1.3$ V

[ESE-2004(EE)]

Q.4 For a logic family

V_{OH} is the minimum output high level voltage
V_{OL} is the maximum output low level voltage
V_{IH} is the minimum acceptable input high level voltage
V_{IL} is the maximum acceptable input low level voltage

The correct relationship among these is:

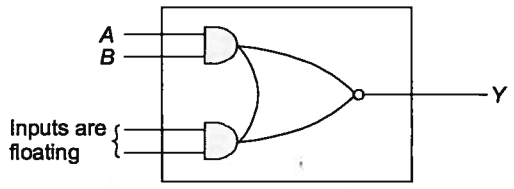
(a) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$
(b) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$
(c) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$
(d) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$ **[ESE-1999]**

Q.5 The open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B and C, D respectively, the output is equal to

(a) $\overline{AB}\,\overline{CD}$ (b) $\overline{AB} + \overline{CD}$
(c) $AB + CD$ (d) $AB \times CD$

[ESE-2002]

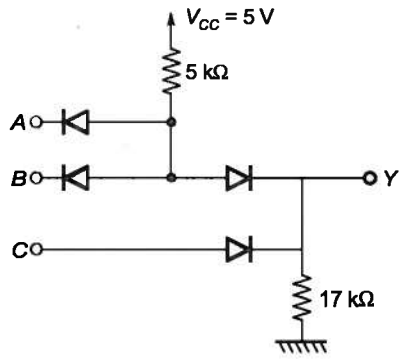
Q.6 The figure shows the internal schematic of a TTL AND-OR-Invert (AOI) gate. For the inputs shown in the figure, the output Y is



(a) 0 (b) 1
(c) AB (d) $\overline{AB}$

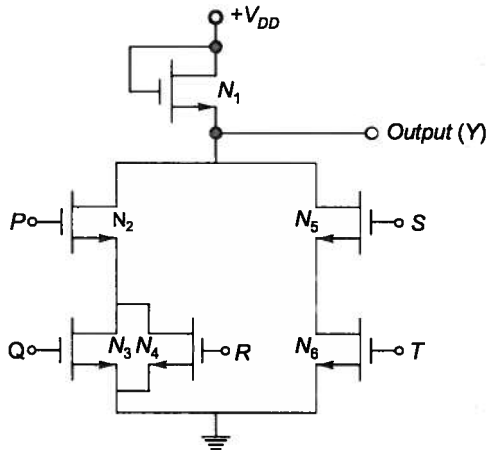
[GATE-2004]

Q.7 The logical expression for the output 'Y' of the diode circuit below is



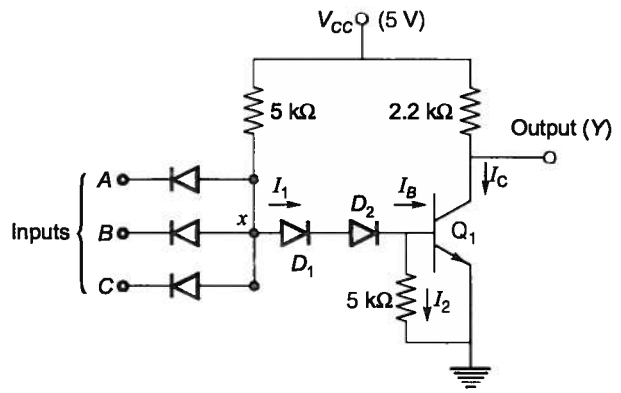
(a) $(A+B)C$ (b) $\overline{A+B}+C$
(c) $(\overline{A+B})C$ (d) $AB+C$

Q.8 An NMOS circuit is shown in the figure below:



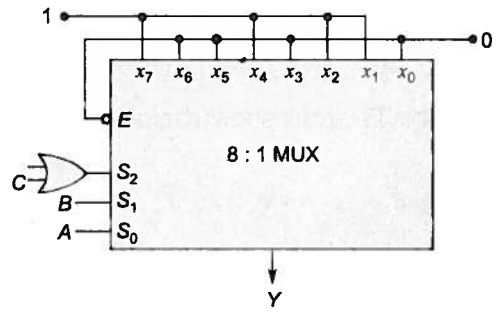
The logical expression for the output (Y) equals to
(a) $\overline{P(Q+R)+ST}$ (b) $P(\overline{Q+R})\cdot ST$
(c) $P+(\overline{QR})(S+T)$ (d) $(\overline{P+Q})R+\overline{S}\,\overline{T}$

Q.9 Consider a DTL circuit as given below:



If all the inputs (A, B, C) are high then,
(a) Input diodes D_1 is ON and D_2 is OFF, Q_1 is in cut-off mode and $Y=\overline{ABC}$.
(b) Input diodes D_1 and D_2 is ON, Q_1 is in active mode and $Y=\overline{A+B+C}$.
(c) Input diodes D_1 and D_2 is ON, Q_1 is in saturation mode and $Y=\overline{ABC}$.
(d) Input diodes D_2 is ON and D_1 is OFF, Q_1 is in saturation and $Y=ABC$.

Q.10 In the TTL circuit in the figure, S_2, S_1 and S_0 are select lines and x_7 and x_0 are input lines. S_0 and x_0 are LSBs. The output Y is



(a) indeterminate (b) $A\oplus B$
(c) $\overline{A\oplus B}$ (d) $\overline{C}(\overline{A\oplus B})+C(A\oplus B)$

[GATE-EC:2001]

Q.11 Which of the following is not a type of output configuration in TTL gates?
(a) Totem-pole output
(b) Open-collector output
(c) Transmission-Gate output
(d) Tri-state output

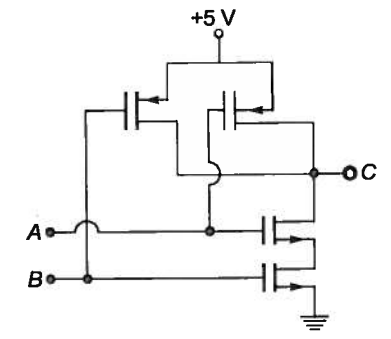
Q.12 The DTL, TTL, ECL and CMOS family of digital ICs are compared in the following 4 columns

	(P)	(Q)	(R)	(S)
Fanout is minimum	DTL	DTL	TTL	CMOS
Power Consumption is minimum	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

The correct column is
(a) P (b) Q
(c) R (d) S

[GATE-EC:2003]

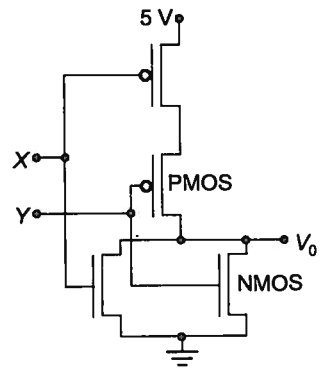
Q.13 Identify the logic gate given in the figure.



(a) NOR (b) NAND
(c) AND (d) OR

[GATE-IN:2005]

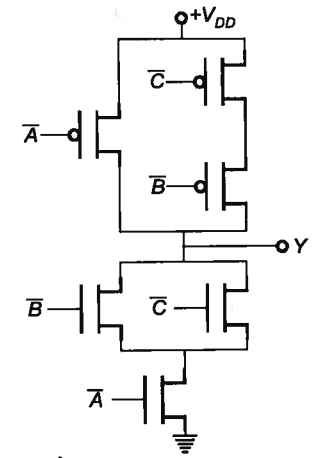
Q.14 A CMOS implementation of a logic gate is shown in the following figure:



The boolean logic function realized by the circuit is
(a) AND (b) NAND
(c) NOR (d) OR

[GATE-IN:2007]

Q.15 The expression for output "Y" for the circuit given below is



(a) $\overline{A}\cdot(\overline{B}+\overline{C})$ (b) $A+BC$
(c) $\overline{A}+\overline{BC}$ (d) $A(B+C)$

Q.16 The switching speed of ECL is very high, because the transistors
(a) are switched between cut-off and saturation region
(b) are switched between active and saturation region
(c) are switched between active and cut-off region
(d) may operate in any of the three regions

Q.17 The figure of merit of a logic family is given by
(a) Gain bandwidth product
(b) (Propagation delay time) × (power dissipation)
(c) (Fan out) × (Propagation delay time)
(d) (Noise-margin) × (Power dissipation)

Q.18 Match **List-I** with **List-II** and select the correct answer using the code given below the Lists:

List-I		List-II
A. HTL	1.	High fan-out
B. CMOS	2.	Highest speed of operation
C. I^2L	3.	High noise immunity
D. ECL	4.	Lowest product of power & delay

Codes:

	A	B	C	D
(a)	3	4	1	2
(b)	2	4	1	3
(c)	3	1	4	2
(d)	2	1	4	3

Numerical Data Type Questions

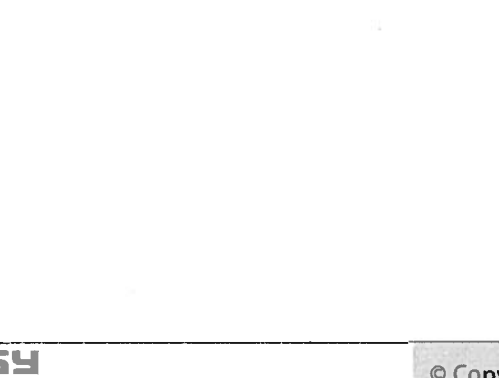
Q.19 The inverter 74 AL S01 has the following specifications:
$I_{OH\,max} = -0.4$ mA, $I_{OL\,max} = 8$ mA,
$I_{IH\,max} = 20$ μA, $I_{ILmax} = -0.1$ mA.
The fan out based on the above will be_____.

Q.20 An IC family has an average propagation delay of 10 ns and an average power dissipation of 5 mW. Figure of merit of IC family is_____ pJ.

Try Yourself

T1. The fan-out of the TTL gate having $I_{OH} = -8$ μA, $I_{IH} = 40$ μA, $I_{OL} = 16$ mA, $I_{IL} = -1.6$ mA is equal to _____.

T2. The transistors used in a portion of the TTL gate shown in the figure have a β = 100. The base-emitter voltage of is 0.7 V for a transistor in active region and 0.75 V for a transistor in saturation. If the sink current I = 1 mA and the output is at logic 0, then the current I_R will be equal to ____mA.



■■■■

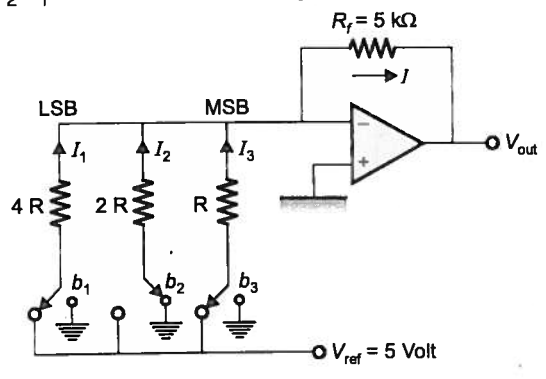
7 ADC and DAC

Multiple Choice Questions

Q.1 The resolution of a 12 bit Analog to Digital converter in percent is
(a) 0.01220 (b) 0.02441
(c) 0.04882 (d) 0.09760
[ESE-2002(EE)]

Q.2 Consider a 6-bit D/A converter having full scale output of 3 mA and a full-scale error of ±0.4% FS. For a binary input sequence of 1 0 1 1 1 1, the range of possible outputs will be
(a) (2220 2240) μA (b) (492 – 512) μA
(c) (2226 – 2250) μA (d)(1295 – 1325) μA

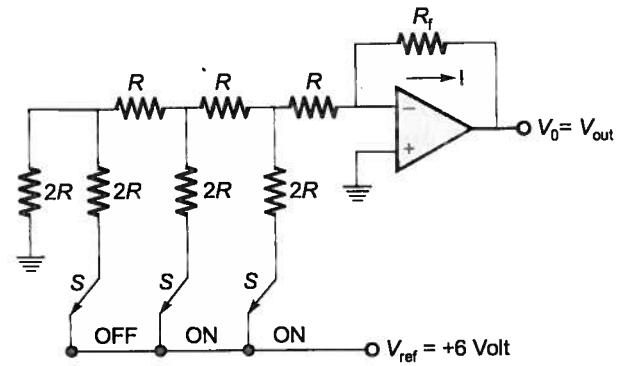
Linked Data for Questions (3 and 4):
A 3-bit weighted resistor D/A converter with MSB resistance R = 10 kΩ having input bit stream $b_3\,b_2\,b_1$ = 1 0 1 is shown in figure below:



Q.3 The total input current 'I' in the circuit will be
(a) 0.125 mA (b) 0.5 mA
(c) 0.625 mA (d) 1.0 mA

Q.4 What is the analog output voltage by this DAC?
(a) –3.125 volt (b) –0.625 volt
(c) –2.5 volt (d) –5.0 volt

Q.5 The circuit shown below is a R-2R ladder type DAC with reference voltage +6 V and R_f = 9 kΩ and R = 1 kΩ.



As above figure-2 switches are ON and 1 is OFF, the output voltage will be
(a) –6.75 V (b) –13.5 V
(c) –20.25 V (d) –40.5 V

Q.6 The output voltage of a 5-bit D/A binary ladder that has a digital input of 11010 (Assuming 0 = 0 V and 1 = +10 V) is
(a) 3.4375 V (b) 6.0 V
(c) 8.125 V (d) 9.6875 V
[ESE-2001]

Q.7 Which one of the following D/A converters has the resolution of approximately 0.4% of its full scale range?
(a) 8-bit (b) 10-bit
(c) 12-bit (d) 16-bit [ESE-2006]

Q.8 An 8 bit successive approximation analog to digital converter has full scale reading of 2.55 V and its conversion time for an analog input of 1 V is 20 μs. The conversion time for a 2 V input will be

(a) 10 μs (b) 20 μs
(c) 40 μs (d) 50 μs

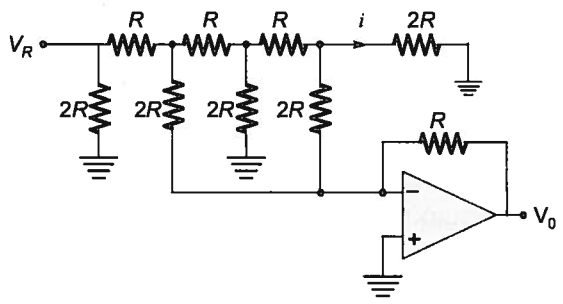
[GATE-2000]

Q.9 The minimum number of comparators required to build an 8 bit flash ADC is
(a) 8 (b) 63
(c) 255 (d) 256

[GATE-2002]

Q.10 4 bit binary weighted resistor *DAC* has *LSB* resistance of 32 kΩ. The corresponding *MSB* resistance is
(a) 2 kΩ (b) 4 kΩ
(c) 8 kΩ (d) 32 kΩ

Statement for Linked Answer Questions (11 and 12):
In the Digital-to-Analog converter circuit shown in the figure below, V_R = 10 V and R = 10 kΩ.



[GATE-EC:2007]

Q.11 The current i is
(a) 31.25 μA (b) 62.5 μA
(c) 125 μA (d) 250 μA

[GATE-EC:2007]

Q.12 The voltage V_0 is
(a) –0.781 V (b) –1.562 V
(c) –3.125 V (d) –6.250 V

[GATE-EC:2007]

Q.13 A 4-bit successive approximation type ADC has a full scale value of 15 V. The sequence of the states, the SAR will traverse, for the conversion of an input of 8.15 V is

(a) Start Conversion → 1000 → 1100 → 1010 → 1001 → 1000 → End Conversion

(b) Start Conversion → 1000 → 0100 → 0010 → 0001 → 0000 → End Conversion

(c) Start Conversion → 1000 → 0100 → 0110 → 0111 → 1000 → End Conversion

(d) Start Conversion → 1000 → 1100 → 1110 → 1111 → 1111 → End Conversion

[GATE-IN:2010]

Q.14 Which of the following statements is/are correct about Analog to Digital converters (ADCs).
(i) Flash type ADCs are fastest
(ii) In successive approximation type ADCs conversion time depends on magnitude of analog voltage.
(iii) Counter type ADCs has fixed conversion time
(iv) Dual-slope type ADCs are slowest
(a) All of these (b) (ii) and (iii)
(c) (i) and (iv) (d) (i) only

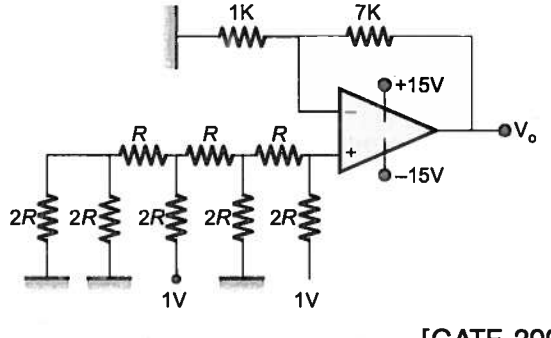
Q.15 For a 4-bit digital to analog convertor, analog voltage varies from 0 to 1.5 volts. The resolution of DAC is
(a) 10 % (b) 6.25 %
(c) 6.67 % (d) 9.375 %

Numerical Data Type Questions

Q.16 An 8-bit D/A converter has a full scale output voltage of 20 V. The output voltage when the input is 11011011, is _____ V.

[ESE-2001]

Q.17 For the 4 bit DAC shown in the figure, the output voltage V_0 is _____ V.



[GATE-2000]

Q.18 A 10-bit DAC provides an analog output which has a maximum value of 10.23 volts. Resolution of the DAC is_____ mV.

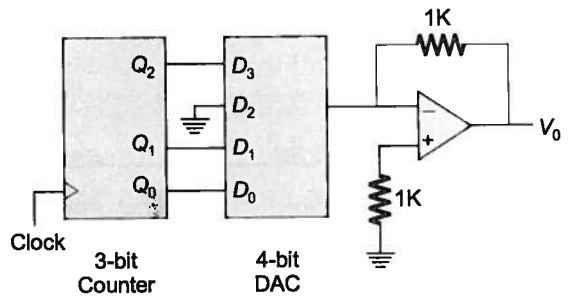
[ESE-2012]

Q.19 The analog output voltage of a 6 bit DAC with reference voltage as 20 V for the digital input 011101 is _____ Volts.

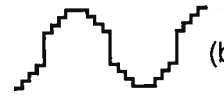
Q.20 A 5 bit D/A converter has a current output. If an output current I_{out} = 10 mA is product for a digital input of 10100, the value of I_{out} for a digital input of 11101 will be_____mA.

Try Yourself

T1. A 4-bit D/A converter is connected to a free-running 3-bit UP counter, as shown in the following figure. Which of the following waveforms will be observed at V_0?



In the figure shown above, the ground has been shown by the symbol ∇.

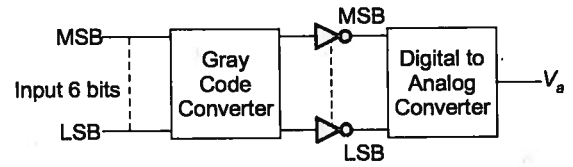
(a) 
(b) 
(c) 
(d) 

[GATE-2006]

T2. A 8-bit A/D convertor is used over a span of zero to 2.56 V. The binary represen-tation of 1.0 V signal is
(a) 011 001 00 (b) 011 100 01
(c) 101 001 01 (d) 101 000 10

[ESE-2013]

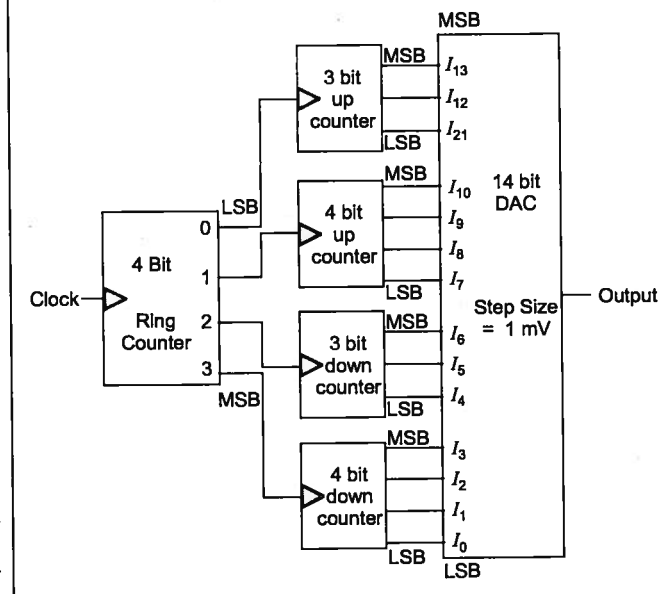
T3. Consider the circuit given below.



The full scale reading of Digital to Analog converter is 10.5 V. Each bit of Gray code converter output is given to digital to analog converter through an invertor. If input to the circuit is 110011, then corresponding output voltage V_a is _____ Volts.

[Ans: 3.45 V]

T4. Consider the system given below:



The clock input is connected to the 4 bit ring counter. The output of the ring counter acts as the clock for the other counters. All the counters shown in figure are positive edge triggered. The output of all counters act as input to a 14 bit DAC with step size (D) equal to 1 mV. If initially all counter are cleared then find the output of DAC after 20 clock pulses.

[Ans: 10.96 V]

2017

MADE EASY

WORKBOOK

Analog Electronics + Digital Electronics + Microprocessors

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8085

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- Importance of Hexa-Decimal Numbers

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- Arithmetical Logical Unit
- Timing and Control unit,

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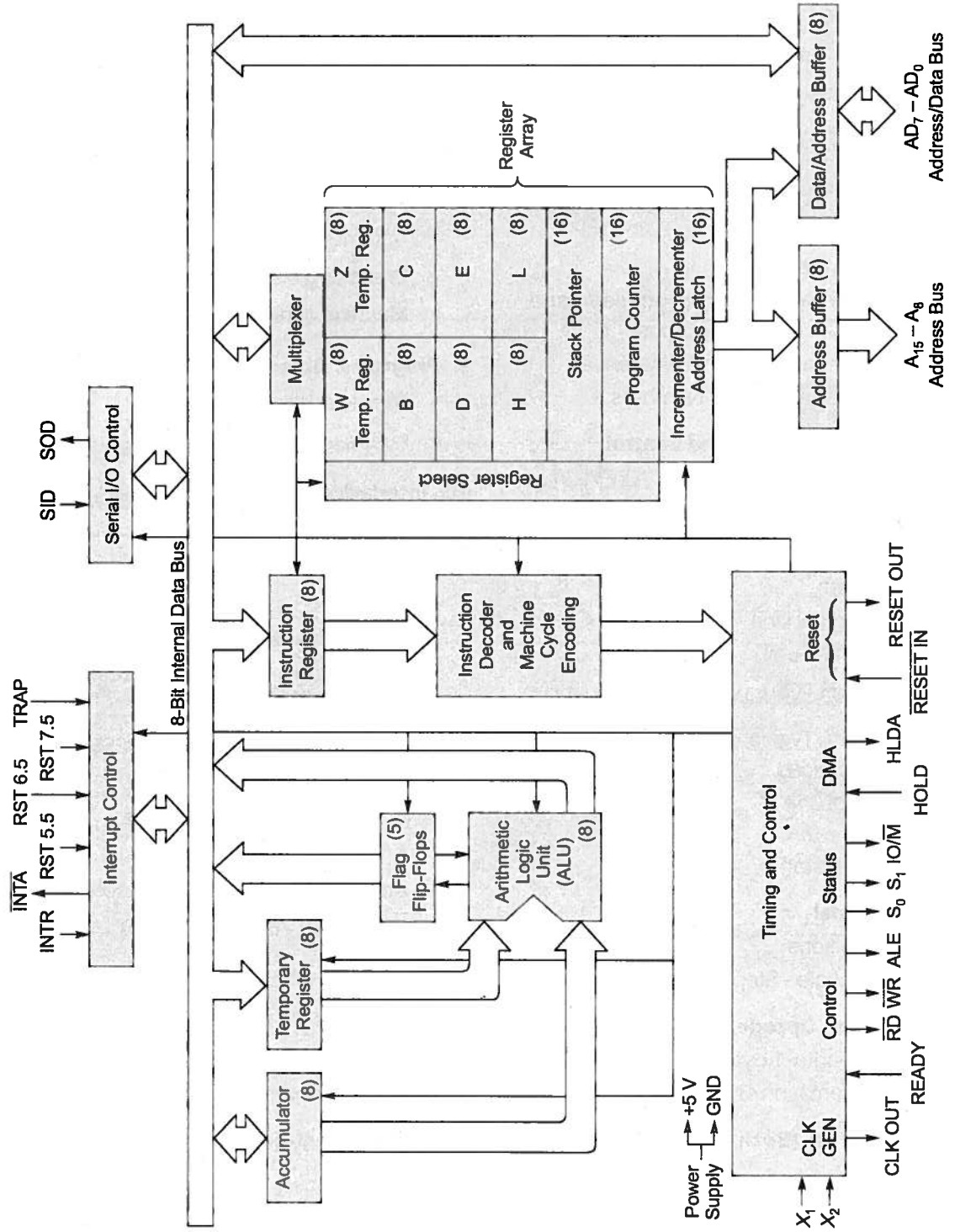
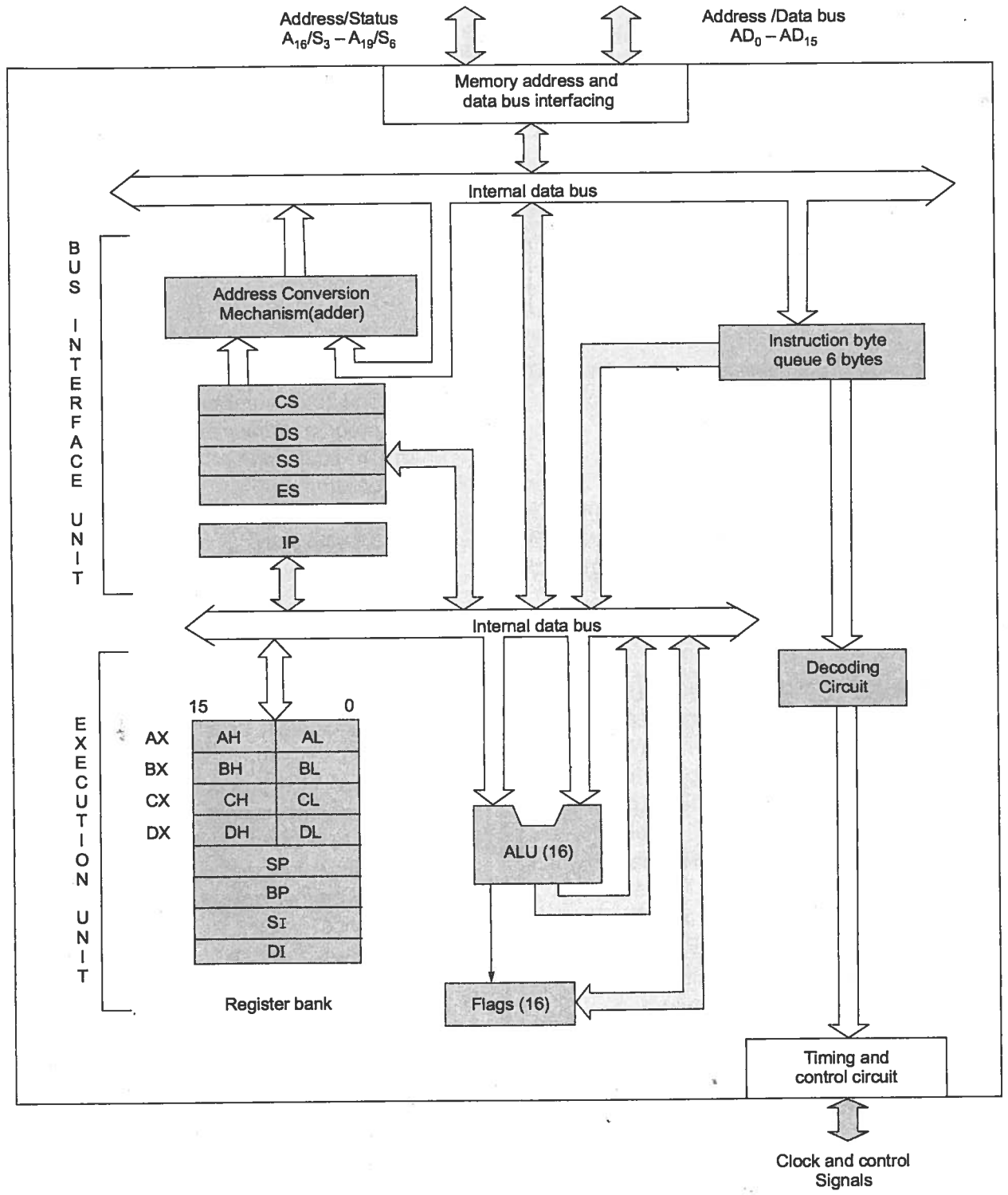
- Definition
- Application



Architecture of INTEL 8085 Microprocessor



Architecture of INTEL 8086 Microprocessor

1 Intel 8085 and Intel 8086

Multiple Choice Questions

Q.1 INTEL 8085 is
(a) 16 bit microprocessor
(b) 32 bit microprocessor
(c) 8 bit microprocessor
(d) 4 bit microprocessor

Q.2 In an 8 bit microcomputer, maximum memory can be connected is 32 K bytes, the length of stack pointer, program counter and number of data lines are respectively
(a) 16, 16, 8 (b) 15, 16, 7
(c) 15, 15, 8 (d) 16, 15, 8

Q.3 For the purpose of data processing an efficient assembly language programmer makes use of the general purpose registers rather than memory. The reason is
(a) The set of instruction for data processing with memory is limited
(b) Data processing becomes easier when register are used
(c) More memory related instructions are required in the program for data processing
(d) Data processing with registers takes fewer cycles than that with memory
[IES-2011]

Q.4 Consider the following statements in 8085 microprocessor data-bus and address bus are multiplexed in order to
1. Increase the speed of microprocessor
2. Reduce the number of pins
3. Connect more peripheral chips

Which of these statements is/are correct ?
(a) 1 only (b) 2 only
(c) 2 and 3 (d) 1, 2 and 3
[IES-2009]

Q.5 The content of the program counter of an 8085 microprocessor is
(a) The total number of instructions in the program already executed
(b) The total number of times a subroutine is called
(c) The memory address of the instruction that is being currently executed
(d) The memory address of the instruction that is to be executed next.
[IES-2010]

Q.6 In an INTEL 8085A microprocessor, why is READY signal used?
(a) To indicate to user that the microprocessor is working and is ready for use
(b) To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device
(c) To slow down a fast peripheral device so as to communicate at the microprocessors device
(d) None of the above **[IES 2008]**

Q.7 In DMA operation, the processor is interfered more in
(a) Cycle stealing technique
(b) Burst mode
(c) Interleaved DMA
(d) None

Q.8 In an 8085 microprocessor, the shift registers which store the result of an addition and the overflow bit are, respectively
(a) B and F (b) A and F
(c) H and F (d) A and C

Q.9 After an arithmetic operation, the flag register of a 8085 microprocessor has the following look :

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	X	1	X	0	X	1

The arithmetic operation has resulted in
(a) A carry and odd parity number having 1 as the MSB
(b) Zero and the auxiliary carry flag being set
(c) A number with even parity and 1 as the MSB
(d) A number with odd parity and 0 as the MSB
[IES-2003]

Q.10 The number of output pins of a 8085 microprocessor are
(a) 40 (b) 27
(c) 21 (d) 19
[IES-2002]

Q.11 Match **List-I(Interrupt)** with **List-II (Property)** and select the correct answer using the code given below the lists:

List-I	List-II
A. RST 7.5	1. Non-maskable
B. RST 5.5	2. Edge sensitive
C. INTR	3. Level sensitive
D. TRAP	4. Non-vectored

Codes :

	A	B	C	D
(a)	1	3	4	2
(b)	2	4	3	1
(c)	1	4	3	2
(d)	2	3	4	1

Q.12 $\overline{\text{INTA}}$ is requried only for
(a) RST 5.5 & RST 6.5
(b) RST 7.5
(c) INTR
(d) TRAP

Q.13 Output of the assembler in machine codes is referred to as
(a) Object program
(b) Source program
(c) Macro instruction
(d) Symbolic addressing **[IES-2003]**

Q.14 The correct sequence of steps in the instruction cycle of a basic computer is
(a) Fetch, Execute, Decode and Read effective address
(b) Read effective address, Decode, Fetch and Execute
(c) Fetch, Decode, Read effective address and Execute
(d) Fetch, Read effective address, Decode and Execute
[IES-2012]

Q.15 Which one of the following cycle is required to fetch and execute an instruction in a 8085 microprocessor ?
(a) Clock cycle (b) Memory cycle
(c) Machine cycle (d) Instruction cycle

Q.16 With referennce to 8085 microprocessor, which of the following statements are correct?
1. INR is 1 byte instruction
2. OUT is 2 byte instruction
3. STA is 3 byte instruction

(a) 1 and 2 only (b) 2 and 3 only
(c) 1 and 3 only (d) 1, 2 and 3

Q.17 For INTEL 8085, match **List-I(Addressing Mode)** with **List-II (Instruction)** and select the correct answer using the code given below the lists:

List-I	List-II
A. Implicit addressing	1. JMP 3FAD H
B. Register-Indirect	2. MOV A, M
C. Immediate	3. LDA 03FC H
D. Direct addressing	4. RAL

Codes:

	A	B	C	D
(a)	4	1	2	3
(b)	4	2	1	3
(c)	3	2	1	4
(d)	3	1	2	4
[IES-2004]

Q.18 Which of the following statements is/are correct?
In INTEL 8085 the interrupt enable flip-flop can be reset by
(*i*) DI instruction.
(*ii*) System RESET.
(*iii*) Interrupt acknowledgment.
(*iv*) SIM instruction.
(a) (*ii*), (*iii*) and (*iv*)
(b) (*ii*) and (*iv*)
(c) (*i*), (*ii*) and (*iii*)
(d) All of these

Q.19 Content of accumulator is 8E H, If SIM instruction is executed, the which of the following statement is true
(a) Serial output data is 1
(b) RST 6.5, 7.5 are enable
(c) RST 5.5 is enable
(d) None of these

Q.20 To have the multiprocessing capabilities of the 8086 microprocessor, the pin connected to the ground is
(a) $\overline{DEN}$ (b) ALE
(c) INTR (d) MN/$\overline{MX}$

Q.21 Effective address is calculated by adding or subtracting displacement value to
(a) immediate address
(b) relative address
(c) absolute address
(d) base address

[IES-2001]

Q.22 In 8086, CS : 907E H, IP : 0FFF H find effective or physical address
(a) 90FFF H (b) 917DF H
(c) FFF09 H (d) None

Numerical Data Type Questions

Q.23 The total number of memory access involved (inclusive of opcode fetch) when an 8085 processor executes the instruction LDA 2016 H is_____.

Q.24 If the clock frequency of a microprocessor is 5 MHz. Then the time required to execute PUSH B instruction is _____ μsec.

Q.25 Consider the execution of the following instruction by a 8085 microprocessor :
LXI H, 01FF H
SHLD 2050 H
After execution the contents of memory locations 2050 H and 2051 H and the registers H and L, will be _____H,_____H,_____H and____H respectively.

Q.26 If the accumulator of the INTEL 8085A microprocessor contians 37 H and the previous operation has set the carry flag, the instruction ACI 56 H will result _____ Hex.

Q.27 If the content of accumulator after execution of RIM is A9H, then interrupt pending is_____ and serial data received is _____.

Conventional Questions

Q.28 Draw and explain architecture and pin diagram of 8085 microprocessor.

Q.29 Draw the timing diagram of OUT 80 H instruction if [A] = 50 H and f_{CLK} = 5 MHz.

Q.30 Explain the sequence of steps involved in CALL and RETURN instruction in 8085.

Q.31 Draw and explain architecture of 8086.

Try Yourself

T1. Explain flag register in 8085 with suitable example.

T2. Explain DMA (Direct memory access) operation in 8085.

T3. The following program starts at locations 0100 H.
LXI SP, 00FF H
LXI H, 0107 H
MVI A, 20 H
SUB M
Find the content of accumulator when the program counter reaches 0109 H is.

[Ans: 00H]

■■■■

2 Programming of Microprocessors

Multiple Choice Questions

Q.1 An 8085 microprocessor executes "STA 1234 H" with starting address location 1FFE H (STA copies the contents of the Accumulator to the 16-bit address location). While the instruction is fetched and executed, the sequence of values written at the address pins $A_{15} - A_8$ is
(a) 1F H, 1F H, 20 H, 12 H
(b) 1F H, FE H, 1F H, FF H, 12 H
(c) 1F H, 1F H, 12 H, 12 H
(d) 1F H, 1F H, 12 H, 20 H, 12 H

[GATE-2014]

Q.2 The stack pointer of an 8085 micro-processor is ABCD H. At the end of execution of the sequence of instructions, what will be the content of the stack pointer?
PUSH PSW
XTHL
PUSH D
JMP FC70 H
(a) ABCB H (b) ABCA H
(c) ABC9 H (d) ABC8 H

[IES-2009]

Q.3 In an 8085 microprocessor, the contents of accumulator, after the following instructions are executed will become
XRA A
MVI B, F0 H
SUB B
(a) 01 H (b) 0F H
(c) F0 H (d) 10 H

Q.4 Consider the following 8085 instructions :
ANA A, ORA A, XRA A, SUB A, CMP A
Now consider the following statements :
1. All are arithmetic and logic instructions
2. All cause the accumulator to be cleared irrespective of its original contents
3. All reset the carry flag
4. All of them are 1 byte instructions
Which of these statements is/are correct ?
(a) 1, 2, 3 and 4 (b) 2 only
(c) 1, 2 and 4 (d) 1, 3 and 4

[IES-2005]

Q.5 Consider the following 8085 microprocessor program
FF00 H : MVI A, DC H
ORA A
LXI H, FF08 H
SUB M
OUT A2 H
HLT
After execution of the command HLT, data displayed at output port A2 H is
(a) 3A H
(b) DC H
(c) A2 H
(d) Can't be determined due to insufficient data

Q.6 Consider the following program to be executed in INTEL 8085 starts at 3000 H
LXI SP, 4000 H
PUSH H
PUSH D
CALL 3050 H
POP H
HLT

After execution of HLT instruction, the program counter and stack pointer contains respectively
(a) 300A H, 3FFC H
(b) 3009 H, 3FFC H
(c) 300A H, 3FFE H
(d) 3009 H, 3FFE H

Q.7 The content of stack pointer and accumulator after the execution of program are respectively
9000 H : LXI SP, FF00H
9003 H : LXI H, 9009H
9006 H : PCHL
9007 H : MVI B, 66H
9009 H : CALL R1
900C H: JMP QUIT
R1: 900F H : XRA A
9010 H : RP
QUIT : 9011 H : HLT
(a) FF00 H, 00 H (b) FEFE H, 0C H
(c) FEFF H, 90 H (d) FE01 H, 66 H

Q.8 Which one of the following 8085 microprocessor programs correctly calculates the product of two 8-bit numbers stored in registers *B* and *C*?

(a)
```
     MVI A, 00 H
     JNZ LOOP
     CMP C
LOOP DCR B
     HLT
```

(b)
```
     MVI, A, 00H
     CMP C
LOOP DCR B
     HLT
```

(c)
```
     MVI A, 00H
LOOP ADD C
     DCR B
     JNZ LOOP
     HLT
```

(d)
```
     MVI A, 00H
     ADD C
     JNZ LOOP
LOOP INR B
     HLT
```

Q.9 Consider the following assembly language program in INTEL 8085.

```
     MVI B, XX H
L2 : DCR B
     JNZ L2
     HLT
```

Find 'XX' if f_{CLK} = 5 MHz and total execution time of program is 500 µs.
(a) B9 H (b) B2 H
(c) 32 H (d) A6 H

Q.10 Consider the following assembly language program in INTEL 8085, if $z = 0$; given

```
     LXI B, 0004 H
L2 : DCX B
     JNZ L2
     HLT
```

How many times the loop L2 is executed ?
(a) Zero (b) 1
(c) 4 (d) Infinite

Q.11 Consider the assembly language program given below

```
(1)          MVI A,  8F H
(2)          SUI   CA H
(3)          JC    DISPLAY
(4)          OUT   PORT1
(5)          HLT
(6) DISPLAY  XRA A
(7)          OUT   PORT1
(8)          HLT
```

If the above program is executed in 8085 then data displayed at PORT 1 and content of flag register is respectively.
(a) 00 H, 95 H (b) C5 H, 95 H
(c) C5 H, 94 H (d) 00 H, 44 H

Q.12 Match **List-I (Instruction)** with **List-II (Application)** and select the correct answer using the code given below :

List-I	List-II
A. SIM	1. 16-bit addition
B. DAD	2. Initializing the stack pointer
C. DAA	3. Serial output data
D. SPHL	4. Checking the current interrupt mask setting
	5. BCD addition

Codes :

	A	B	C	D
(a)	5	4	2	1
(b)	4	1	5	2
(c)	5	1	2	4
(d)	3	4	5	1

Numerical Data Type Questions

Q.13 LXI H, 9876 H
SHLD 5000 H
MOV A, M
STA 4000 H
HLT
Length of the program is _____ bytes.

Q.14 Consider the following assembly language program in INTEL 8085.

```
     XRA A
     LXI B,  000F H
LOOP DCX B
     ANI   FF H
     JC    LOOP
     HLT
```

While execution of above program the loop will be executed _____ times.

Q.15 Consider the following assembly language program in INTEL 8085.

```
     MVI C, 00 H
L3 : DCR C
     JNZ L3
     HLT
```

How many times the instructions DCR C is executed_____.

Q.16 Consider the following assembly language program in INTEL 8085.

```
     MVI A, 1C H
     ORA A
L1 : RAL
     JNC L1
     HLT
```

f_{CLK} = 2 MHz, then time for which loop executes is_____µsec.

Q.17 Consider the assembly language program given below.

```
MVI A, 84 H
MVI B, AB H
SUB B
MOV D, A
HLT
```

If 8085 is operating at a frequency of 3 MHz then total time required to execute the above program _____µsec.

Q.18 Consider the program given below for INTEL 8085

```
     MVI C, 0B H
     LXI H, 2400 H
     LXI D, 3400 H
LOOP MOV A, M
     STAX D
     INR L
     INR E
     DCR C
     JNZ LOOP
     HLT
```

The total number of memory accesses required are _____.

Q.19 Consider the following 8085 microprocessor assembly language program.

```
1. LXI SP, 0200 H
2. LXI B, 1028 H
3. LXI H, 42FF H
4. PUSH H
5. LXI D, 20FE H
6. DAD B
7. X CHG
8. DAD D
9. HLT
```

After execution of above program content of HL register pair is _____ hex.

Conventional Questions

Q.20 Write an assembly language program to transfers 5 bytes of data from location 5000 H to 9000 H in INTEL 8085.

Q.21 Write on assembly language program to find number of even and odd number from *n* bytes of data . Store the count of even numbers in *B* and odd numbers in *C*.

Q.22 Write an ALP to find smallest number from 10 bytes of data.

Q.23 Write an assembly language program to generate a delay of 100 msec in INTEL 8085.

Try Yourself

T1. Consider the following assembly language program

```
        XRA A
        MVI A, 50 H
        MVI B, 0F H
LOOP    DCR A
        JNZ LOOP
        INR B
        JC LOOP
        HLT
```

The program is executed in INTEL 8085, find the number of times INR B executed.

[Ans: 1]

T2. Consider the following 8085 microprocessor program

```
    MVI C, FF H
    MVI B, FF H
L1 : DCR C
    JNZ L1
    DCR B
    JNZ L1
    HLT
```

How many times DCR C instruction executes?

[Ans: 65,279]

T3. Consider the following instructions executed in 8086

```
PUSH AX; AX has 0020H in it
PUSH BX; BX has 1234H in it
POP AX;
ADD AX, BX;
POP CX
```

Find the content of CX register after execution.

[Ans: 20 H]

■■■■

3 Memory and I/O Interfacing

Multiple Choice Questions

Q.1 RAM and ROM, both are
(a) Sequentially accessed memory
(b) Randomly accessed memory
(c) Either (a) or (b)
(d) RAM: Randomly accessed, ROM sequentially accessed

Q.2 Memory chips of four different sizes as below are available :
1. 32 K × 4
2. 32 K × 16
3. 8 K × 8
4. 16 K × 4

All the memory chips as mentioned in the above list are Read/Write memory. What minimal combination of chips alone can map full address space of 8085 microprocessor?
(a) 1 and 2 (b) 1 only
(c) 2 only (d) 4 only

[IES-2005]

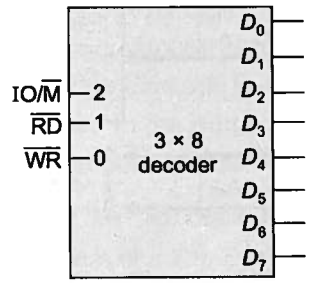
Q.3 A memory of 8 KB is designed using 2048 × 8 RAM chips. The number of chips required are
(a) 4 (b) 6
(c) 8 (d) 16

Q.4 In a 512 × 4 ROM chip, the number of address lines are
(a) 512 (b) 4
(c) 9 (d) 11

Q.5 Which of the following components are used in interfacing memory with microprocessor
(a) Tristate buffer (b) Encoder
(c) Latch (d) All of the above

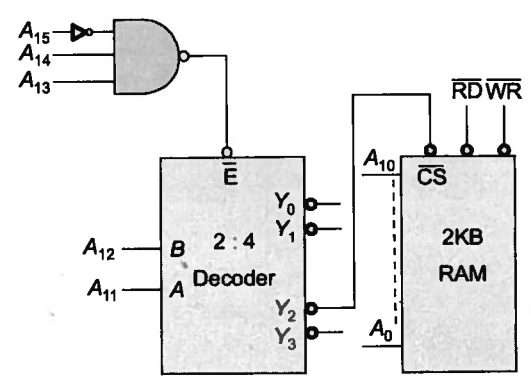
Q.6 Ending address of an 8 KB ROM is B72E H find starting address
(a) D72D H (b) 972F H
(c) 6543 H (d) None

Q.7 Consider the 3 × 8 decoder given below



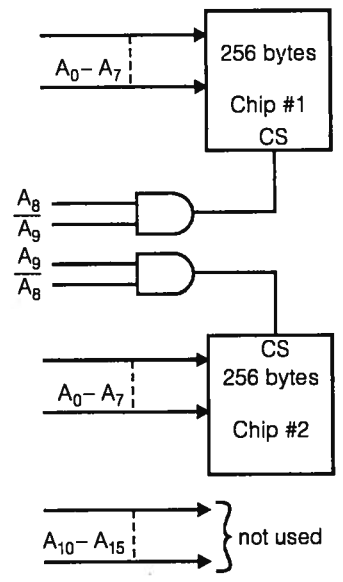
If this to be used with 8085 to generate read and write control signals then valid outputs are
(a) $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$
(b) $D_0, D_1, D_2, D_4, D_5, D_6$
(c) D_1, D_2, D_5, D_6
(d) D_0, D_3, D_4, D_7

Q.8 Memory map of given interfacing logic is



(a) 6800 H - 6FFF H
(b) 7800 H - 7FFF H
(c) 7000 H - 77FF H
(d) None

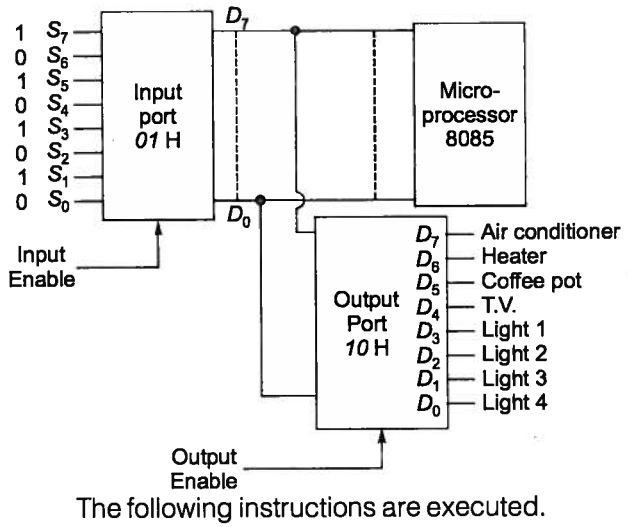
Q.9 What memory address range is NOT represented by chip#1 and chip #2 in the figure. A_0 to A_{15} in this figure are the address lines and CS means Chip select.



(a) 0100-02FF (b) 1500-16FF
(c) F900-FAFF (d) F800-F9FF

[GATE-2005]

Q.10 Consider the figure given below.



The following instructions are executed.

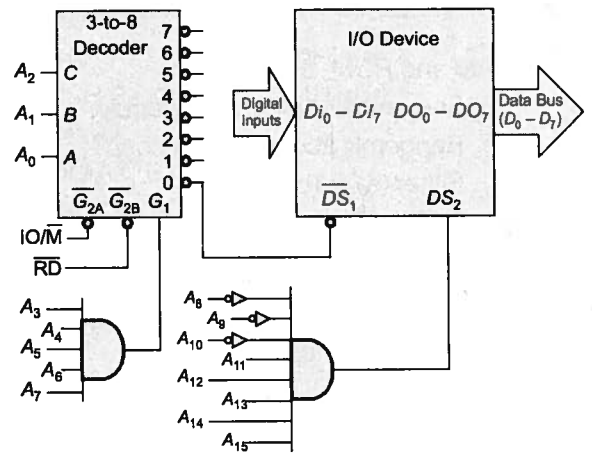
IN 01 H
XRI C2 H
RAL
OUT 10 H

Which of the following statements is/are true.

(*i*) Air conditioner and coffee pot are ON.
(*ii*) Heater and T.V. are ON.
(*iii*) Only 2 Lights are ON.
(*iv*) T.V. and only Light 4 are ON.

(a) (*ii*) and (*i*) (b) (*ii*) only
(c) (*iii*) and (*iv*) (d) (*ii*) and (*iv*)

Q.11 For the 8085 microprocessor, the interfacing circuit to input 8-bit digital data ($DI_0 - DI_7$) from an external device is shown in the figure. The instruction for correct data transfer is



(a) MVI A, F8 H (b) IN F8 H
(c) OUT F8 H (d) LDA F8F8 H

[2014 : 2 Marks, Set-2]

Q.12 The following is not true for RS232 standards
(a) It establishes the way data is coded
(b) It defines signal voltage levels
(c) Does not decide data transmission rate
(d) It defines standard connector configurations

Q.13 The interfacing device used to generate accurate time delay in a microcomputer system is
(a) INTEL 8251 (b) INTEL 8253
(c) INTEL 8257 (d) INTEL 8259

Q.14 What is the maximum memory that can be interfaced with INTEL 8086?
(a) 64 KB (b) 1 MB
(c) 8 KB (d) 2 MB

Numerical Data Type Questions

Q.15 The internal memory of INTEL 8085 is_____byte.

Q.16 Maximum number of 256 × 4 memory chips that can be interfaced with INTEL 8085 microprocessor are _____.

Q.17 A read write memory chip has a capacity of 32 kb. If the memory chip is having equal number address lines and data lines, then minimum number of data lines are _____.

Q.18 A memory system of 128 K bytes needs to be designed with RAM chips of 2 K bytes each and a decoder circuitry constructed with 1 × 2 decoder chips with "enable" input. The minimum number of decoder chips required in design are _____.

Q.19 In INTEL 8085, suppose the peripheral mapped I/O has address length of M and memory mapped I/O has address length of N. Then M + N = _____.

Conventional Questions

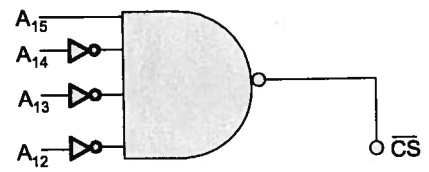
Q.20 Describe various interfacing components.

Q.21 Design a memory of 8 KB using 2048 × 8 RAM chips such that the memory map is 2000 H to 3 FFFH.

Q.22 What are the differences between memory mapped I/O and I/O mapped I/O?

Q.23 Write an ALP to access a data byte from port address 60 H and send it to port address 70 H where a display is connected. Draw the required interfacing logic circuit.

Q.24 If the output of the NAND gate is connected to a memory chip $\overline{CS}$ line then find the capacity and memory map of the memory chip.

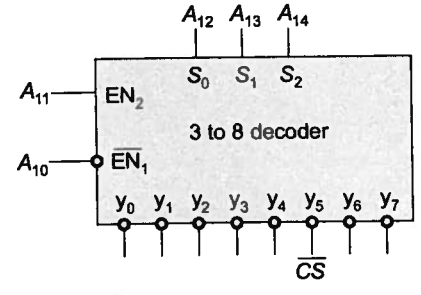


Try Yourself

T1. If a page of memory is assumed to be 256 bytes then in how many pages total memory of 8085 can be treated ?

[Ans: 256]

T2. A 1 Kbyte memory module has to be interfaced with an 8-bit microprocessor that has 16 address lines. The address lines A_0 to A_9 of the processor are connected to the corresponding address lines of the memory module. The active low chip select $\overline{CS}$ of the memory module is connected to the y_5 output of a 3 to 8 decoder with active low outputs. S_0, S_1, and S_2 are the input lines to the decoder, with S_2 as the MSB. The decoder has one active low $\overline{EN_1}$ and one active high EN_2 enable lines as shown below. The address range(s) that gets mapped onto this memory module is (are)



(a) 3000_H to $33FF_H$ and $E000_H$ to $E3FF_H$
(b) 1400_H to $17FF_H$
(c) 5300_H to $53FF_H$ and $A300_H$ to $A3FF_H$
(d) 5800_H to $5BFF_H$ and $D800_H$ to $DBFF_H$

[Ans: (d)]